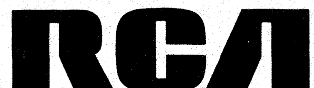

RRF Power MOSFETs

Replacements for International Rectifier IRF types

IRF 513

RRF 513

Replacements for International Rectifier IRF Types

The New RCA RRF series of Power MOSFETs are more then just industry drop-ins! This new series offers the most advanced state-of-the-art technological breakthroughs in design, processing, and electrical features available in the industry today.

- Over 850,000 active hexagonal cells per square inch.
- Process disciplines similar to those of 3-micron QMOS Integrated Circuits.
- 125-MM wafer facility.
- Fully automated wafer transfer and handling capability.
- Fully automated TO-3 and TO-220 assembly line, capable of producing over 10M units per month.
- 100% automated electrical testing of pellet and finished device.
- Plasma-etching of polysilicon and oxide films.
- Direct step on wafer-projection lithography.
- ION implantation (low and high dose).
- Class 100 computer-controlled diffusion room.
- Perform in-line HTRB wafer reliability tests.
- Short-duration accelerated-stress testing, power cycling, bias life.
- AOQ $<$ 50 ppm.
- Competitive pricing and delivery (4 to 12 weeks) thats our commitment!
- Power MOSFET spice modeling and applications hot-line (1-800-RCA-APPL)

RCA is dedicated to becoming a leading supplier of Power MOSFETS and will continue to offer most advanced technology devices at affordable prices. Look at our record since 1982, this only shows part of RCA's commitment to Power MOSFETS, there are many new and exciting programs we plan to announce soon. We invite your inquires.

Our broad-based Power MOSFET line includes:

- Conventional 10V gate N-Channels
- Conventional 10V Gate P-Channels
- Logic-Level-FET, 5V Gate N-Channel
- TO-218 Plastic TO-3
- "RRF" Industry Types
- "2N" JEDEC QPL Types
- "COMFET" High Speed $<$ 200NS TOFF
- "COMFET" Slow Speed $<$ 2.OUS TOFF

This book contains detailed technical data on the RRF series of Power MOSFETs. Similar information on other RCA Power MOSFET products is provided in the RCA Catalog, **Power MOSFETs,** PMP-411A.

RCA Solid State | Somerville, NJ • Brussels • Paris • London
Hamburg • Sao Paulo • Hong Kong

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When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

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Power MOSFETs

RCA Equivalents to IRF Types

RCA Type	Package	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS}(on)$ Ohms
RRFF110	TO-205AF	3.5	100	15	0.60
RRFF111	TO-205AF	3.5	60	15	0.60
RRFF112	TO-205AF	3.0	100	15	0.80
RRFF113	TO-205AF	3.0	60	15	0.80
RRFF120	TO-205AF	6.0	100	20	0.30
RRFF121	TO-205AF	6.0	60	20	0.30
RRFF122	TO-205AF	5.0	100	20	0.40
RRFF123	TO-205AF	5.0	60	20	0.40
RRFF130	TO-205AF	8.0	100	25	0.18
RRFF131	TO-205AF	8.0	60	25	0.18
RRFF132	TO-205AF	7.0	100	25	0.25
RRFF133	TO-205AF	7.0	60	25	0.25
RRF120	TO-204AA	8.0	100	40	0.30
RRF121	TO-204AA	8.0	60	40	0.30
RRF122	TO-204AA	7.0	100	40	0.40
RRF123	TO-204AA	7.0	60	40	0.40
RRF130	TO-204AA	14.0	100	75	0.18
RRF131	TO-204AA	14.0	60	75	0.18
RRF132	TO-204AA	12.0	100	75	0.25
RRF133	TO-204AA	12.0	60	75	0.25
RRF220	TO-204AA	5.0	200	40	0.80
RRF221	TO-204AA	5.0	150	40	0.80
RRF222	TO-204AA	4.0	200	40	1.20
RRF223	TO-204AA	4.0	150	40	1.20
RRF230	TO-204AA	9.0	200	75	0.40
RRF231	TO-204AA	9.0	150	75	0.40
RRF232	TO-204AA	8.0	200	75	0.60
RRF233	TO-204AA	8.0	150	75	0.60
RRF241	TO-204AE	18.0	150	75	0.18
RRF243	TO-204AE	16.0	150	75	0.22
RRF251	TO-204AE	30.0	150	150	0.085
RRF253	TO-204AE	25.0	150	150	0.12
RRF320	TO-204AA	3.0	400	40	1.80
RRF321	TO-204AA	3.0	350	40	1.80
RRF322	TO-204AA	2.5	400	40	2.50
RRF323	TO-204AA	2.5	350	40	2.50
RRF330	TO-204AA	5.5	400	75	1.00
RRF331	TO-204AA	5.5	350	75	1.00
RRF332	TO-204AA	4.5	400	75	1.50
RRF333	TO-204AA	4.5	350	75	1.50
RRF420	TO-204AA	2.5	500	40	3.00
RRF421	TO-204AA	2.5	450	40	3.00
RRF422	TO-204AA	2.0	500	40	4.00
RRF423	TO-204AA	2.0	450	40	4.00

RCA Type	Package	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS}(on)$ Ohms
RRF430	TO-204AA	4.5	500	75	1.50
RRF431	TO-204AA	4.5	450	75	1.50
RRF432	TO-204AA	4.0	500	75	2.00
RRF433	TO-204AA	4.0	450	75	2.00
RRF510	TO-220AB	4.0	100	20	0.60
RRF511	TO-220AB	4.0	60	20	0.60
RRF512	TO-220AB	3.5	100	20	0.80
RRF513	TO-220AB	3.5	60	20	0.80
RRF520	TO-220AB	8.0	100	40	0.30
RRF521	TO-220AB	8.0	60	40	0.30
RRF522	TO-220AB	7.0	100	40	0.40
RRF523	TO-220AB	7.0	60	40	0.40
RRF530	TO-220AB	14.0	100	75	0.18
RRF531	TO-220AB	14.0	60	75	0.18
RRF532	TO-220AB	12.0	100	75	0.25
RRF533	TO-220AB	12.0	60	75	0.25
RRF610	TO-220AB	2.5	200	20	1.50
RRF611	TO-220AB	2.5	150	20	1.50
RRF612	TO-220AB	2.0	200	20	2.40
RRF613	TO-220AB	2.0	150	20	2.40
RRF620	TO-220AB	5.0	200	40	0.80
RRF621	TO-220AB	5.0	150	40	0.80
RRF622	TO-220AB	4.0	200	40	1.20
RRF623	TO-220AB	4.0	150	40	1.20
RRF630	TO-220AB	9.0	200	75	0.40
RRF631	TO-220AB	9.0	150	75	0.40
RRF632	TO-220AB	8.0	200	75	0.60
RRF633	TO-220AB	8.0	150	75	0.60
RRF641	TO-220AB	18.0	150	125	0.18
RRF643	TO-220AB	16.0	150	125	0.22
RRF720	TO-220AB	3.0	400	40	1.80
RRF721	TO-220AB	3.0	350	40	1.80
RRF722	TO-220AB	2.5	400	40	2.50
RRF723	TO-220AB	2.5	350	40	2.50
RRF730	TO-220AB	5.5	400	75	1.00
RRF731	TO-220AB	5.5	350	75	1.00
RRF732	TO-220AB	4.5	400	75	1.50
RRF733	TO-220AB	4.5	350	75	1.50
RRF820	TO-220AB	2.5	500	40	3.00
RRF821	TO-220AB	2.5	450	40	3.00
RRF822	TO-220AB	2.0	500	40	4.00
RRF823	TO-220AB	2.0	450	40	4.00
RRF830	TO-220AB	4.5	500	75	1.50
RRF831	TO-220AB	4.5	450	75	1.50
RRF832	TO-220AB	4.0	500	75	2.00
RRF833	TO-220AB	4.0	450	75	2.00

JEDEC Types

RCA Type	Package	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS}(on)$ Ohms
2N6755	TO-204AA	12.0	60	75	0.25
2N6756	TO-204AA	14.0	100	75	0.18
2N6757	TO-204AA	8.0	150	75	0.60
2N6758	TO-204AA	9.0	200	75	0.40
2N6759	TO-204AA	4.5	350	75	1.50
2N6760	TO-204AA	5.5	400	75	1.00
2N6761	TO-204AA	4.0	450	75	2.00
2N6762	TO-204AA	4.5	500	75	1.50

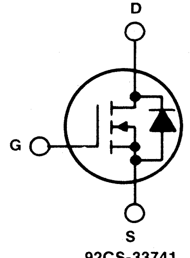
RCA Type	Package	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS}(on)$ Ohms
2N6764	TO-204AE	38.0	100	150	0.055
2N6766	TO-204AE	30.0	200	150	0.085
2N6782	TO-205AF	3.5	100	15	0.60
2N6788	TO-205AF	6.0	100	20	0.30
2N6796	TO-205AF	8.0	100	25	0.18

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



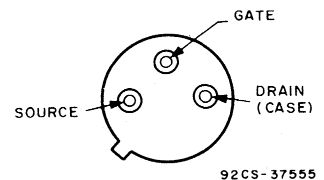
N-CHANNEL ENHANCEMENT MODE

The RRFF110, RRFF111, RRFF112 and RRFF113* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

*These devices are equivalent to International Rectifier Power MOSFETs IRFF110, IRFF111, IRFF112 and IRFF113, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-205AF

Absolute Maximum Ratings

	Parameter	RRFF110	RRFF111	RRFF112	RRFF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 14	14	12	12	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRFF110 RRFF112	100	–	–	V	V_{GS} = 0V
		RRFF111 RRFF113	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRFF110 RRFF111	3.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRFF112 RRFF113	3.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRFF110 RRFF111	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		RRFF112 RRFF113	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRFF110 RRFF111	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRFF112 RRFF113	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRFF110 RRFF111	–	–	14	A	
		RRFF112 RRFF113	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	RRFF110 RRFF111	–	–	2.5	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		RRFF112 RRFF113	–	–	2.0	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	200	–	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.0	–	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

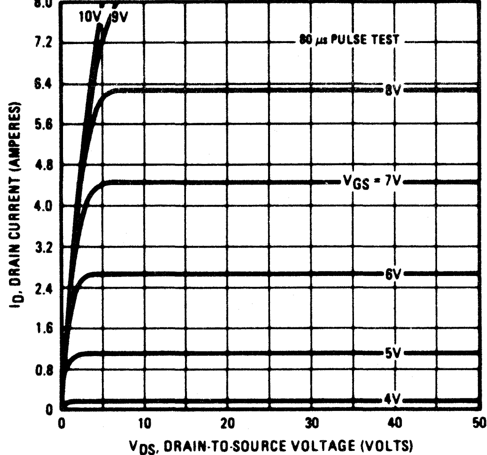


Fig. 1 — Typical Output Characteristics

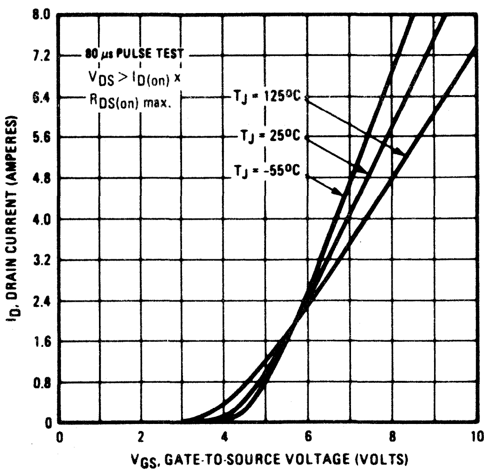


Fig. 2 — Typical Transfer Characteristics

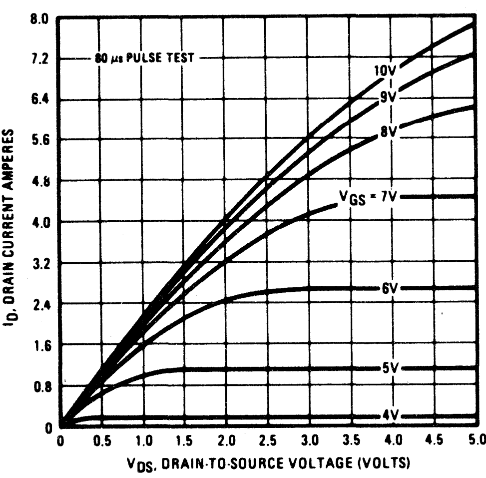


Fig. 3 — Typical Saturation Characteristics

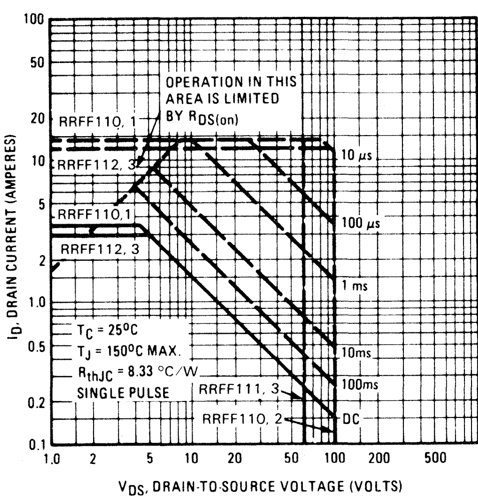


Fig. 4 — Maximum Safe Operating Area

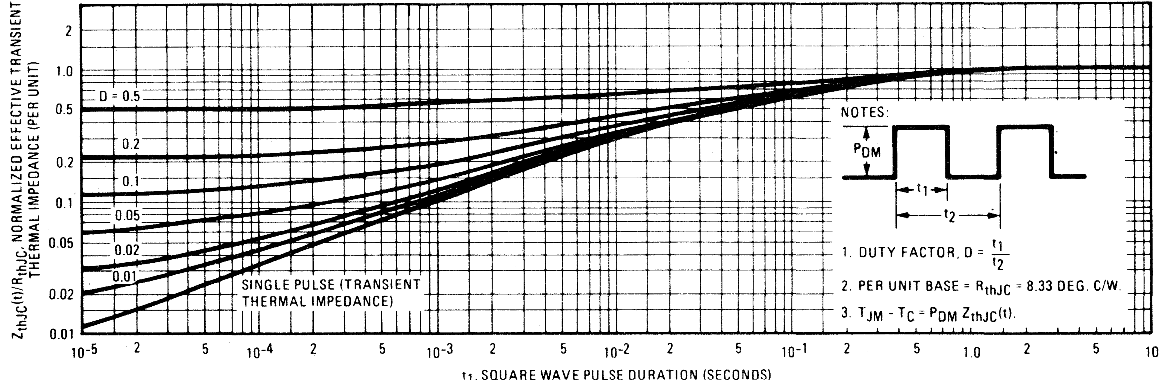


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

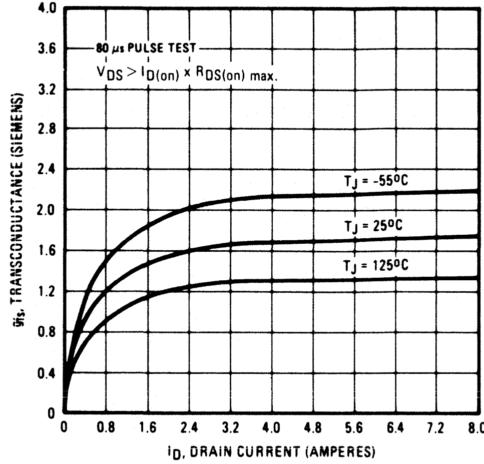


Fig. 6 — Typical Transconductance Vs. Drain Current

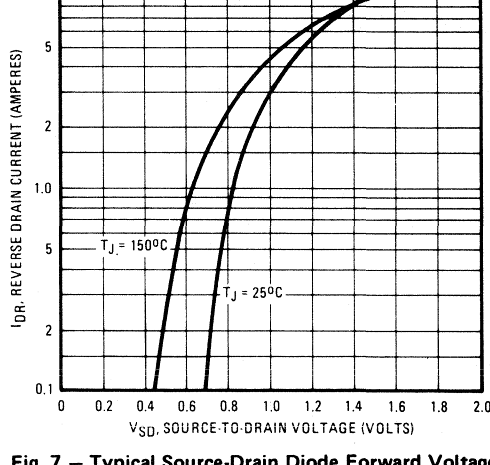


Fig. 7 — Typical Source-Drain Diode Forward Voltage

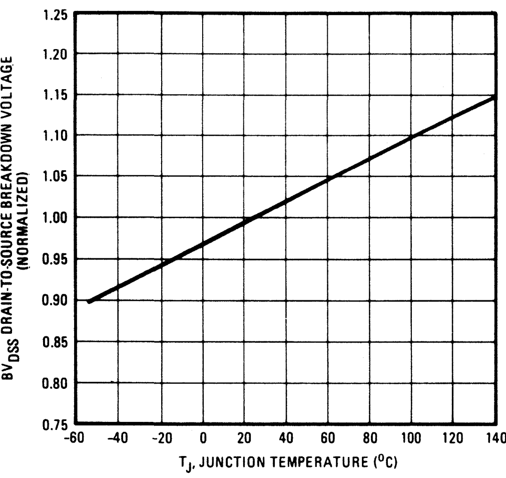


Fig. 8 — Breakdown Voltage Vs. Temperature

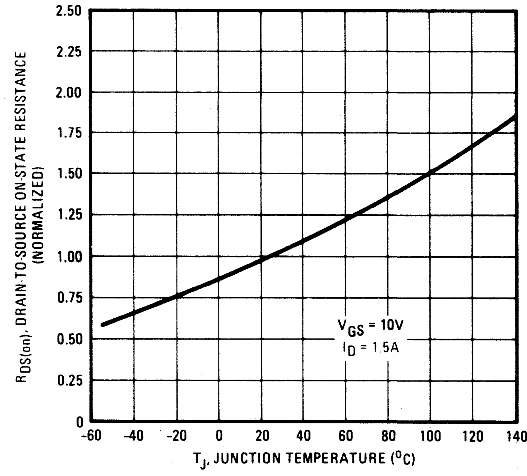


Fig. 9 — Normalized On-Resistance Vs. Temperature

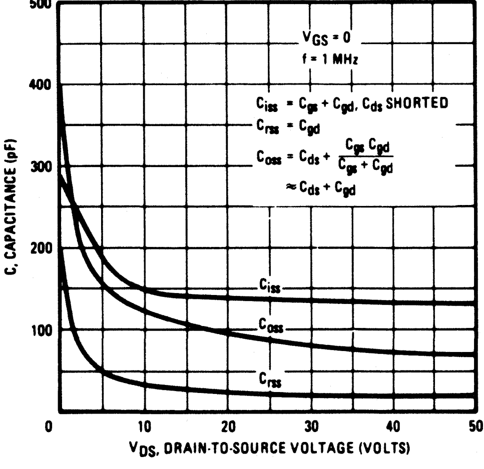


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

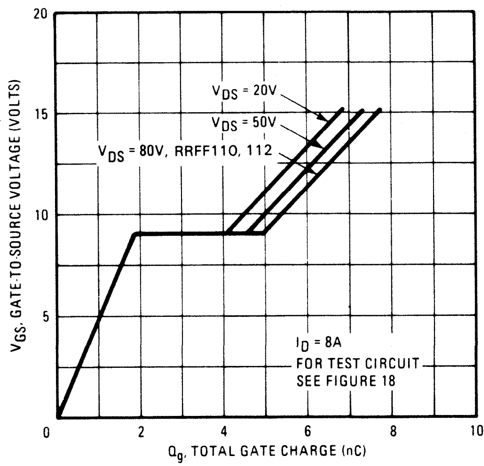


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

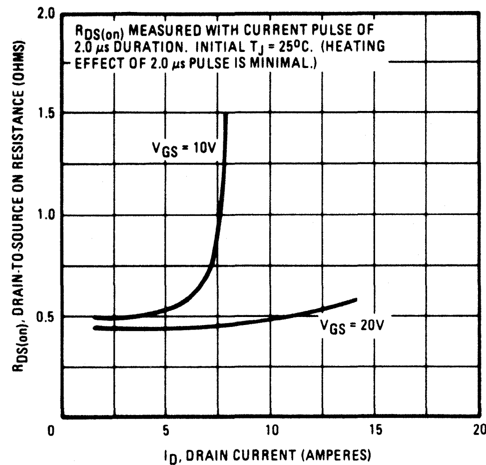


Fig. 12 – Typical On-Resistance Vs. Drain Current

Fig. 13 – Maximum Drain Current Vs. Case Temperature

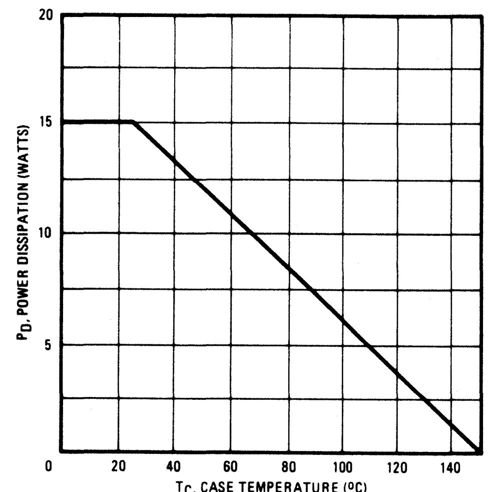


Fig. 14 – Power Vs. Temperature Derating Curve

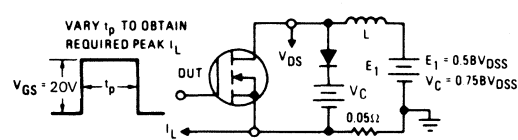


Fig. 15 – Clamped Inductive Test Circuit

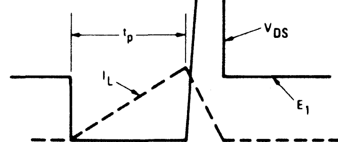


Fig. 16 – Clamped Inductive Waveforms

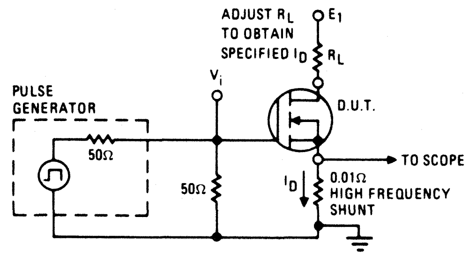


Fig. 17 – Switching Time Test Circuit

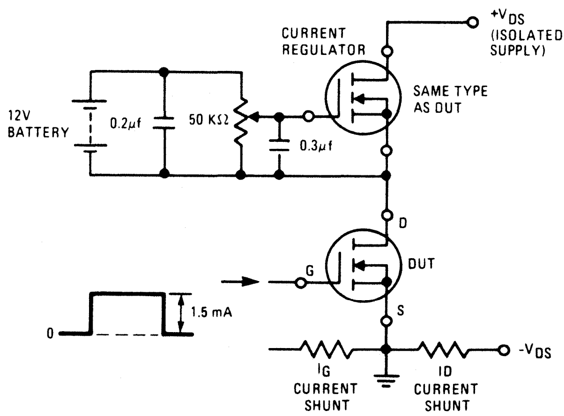


Fig. 18 – Gate Charge Test Circuit

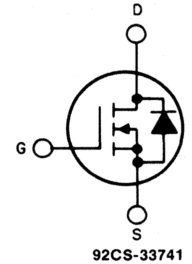
N-Channel Enhancement-Mode Power Field-Effect Transistors

5.0A and 6.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



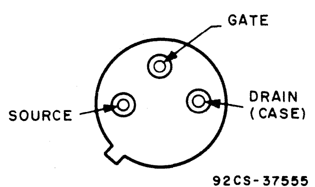
N-CHANNEL ENHANCEMENT MODE

The RRFF120, RRFF121, RRFF122 and RRFF123* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

*These devices are equivalent to International Rectifier Power MOSFETs IRFF120, IRFF121, IRFF122 and IRFF123, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-205AF

Absolute Maximum Ratings

	Parameter	RRFF120	RRFF121	RRFF122	RRFF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	24	24	20	20	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRFF120 RRFF122	100	–	–	V	V_{GS} = 0V
		RRFF121 RRFF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRFF120 RRFF121	6.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRFF122 RRFF123	5.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRFF120 RRFF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		RRFF122 RRFF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	37	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRFF120 RRFF121	–	–	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRFF122 RRFF123	–	–	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRFF120 RRFF121	–	–	24	A	
		RRFF122 RRFF123	–	–	20	A	
V_{SD}	Diode Forward Voltage ②	RRFF120 RRFF121	–	–	2.5	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
		RRFF122 RRFF123	–	–	2.3	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.2	–	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

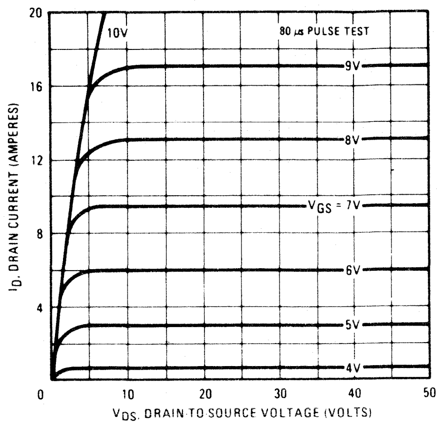


Fig. 1 — Typical Output Characteristics

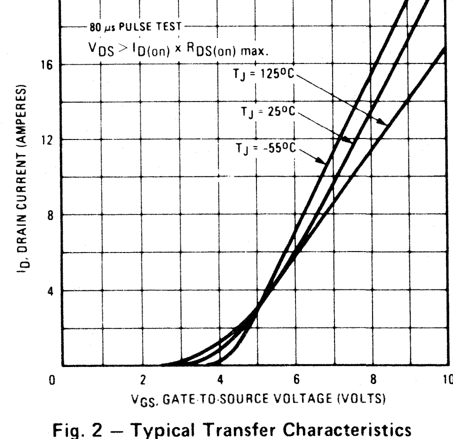


Fig. 2 — Typical Transfer Characteristics

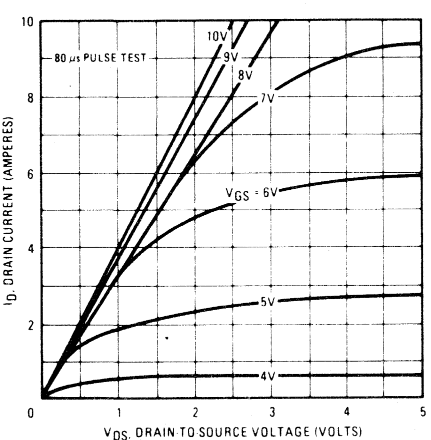


Fig. 3 — Typical Saturation Characteristics

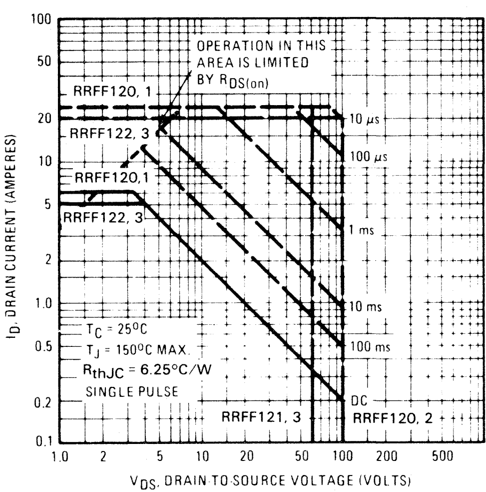


Fig. 4 — Maximum Safe Operating Area

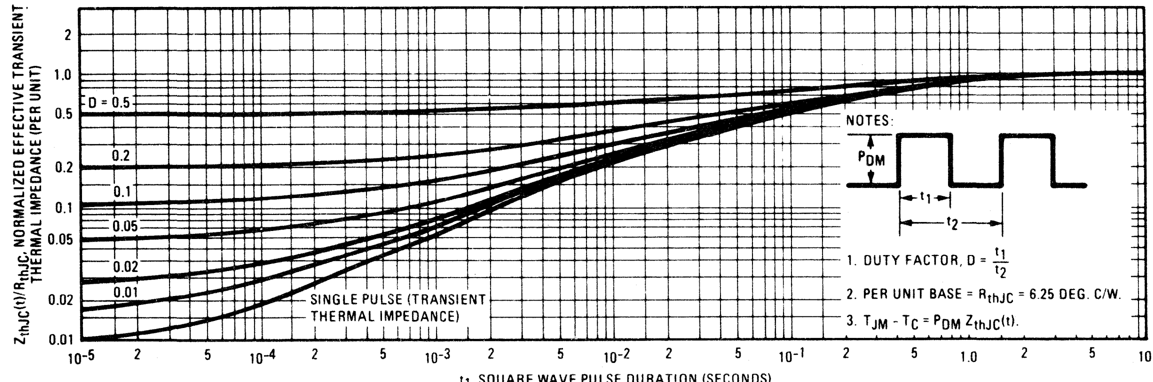


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

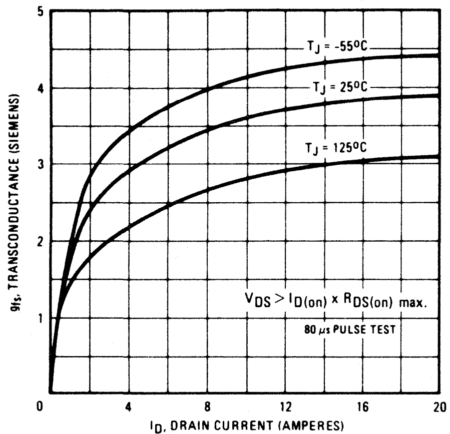


Fig. 6 — Typical Transconductance Vs. Drain Current

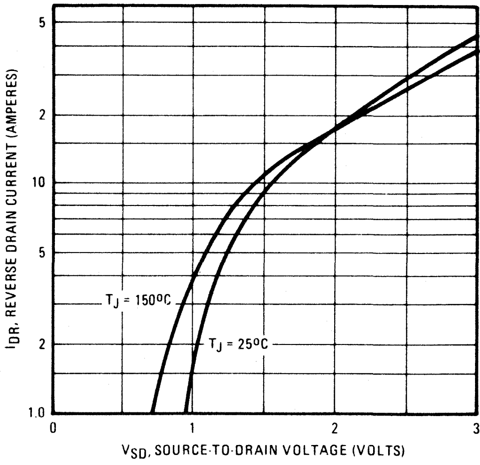


Fig. 7 — Typical Source-Drain Diode Forward Voltage

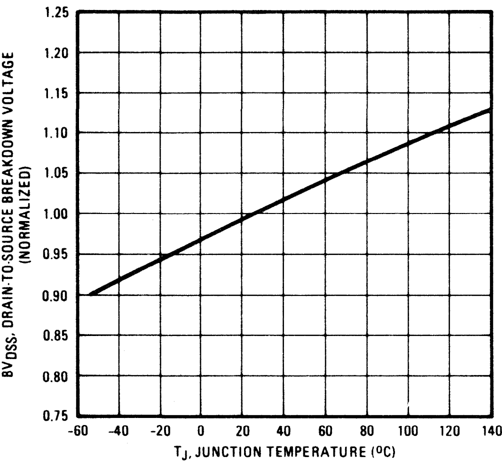


Fig. 8 — Breakdown Voltage Vs. Temperature

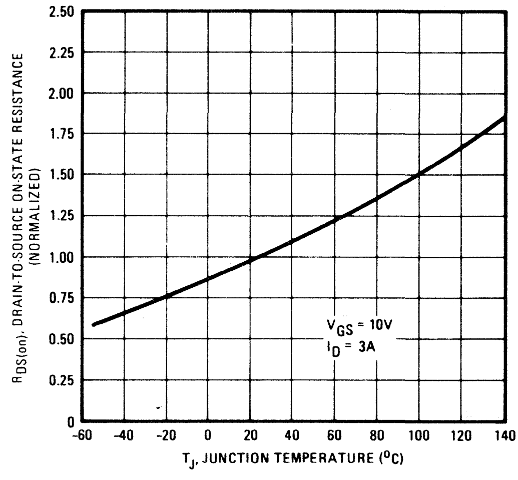


Fig. 9 — Normalized On-Resistance Vs. Temperature

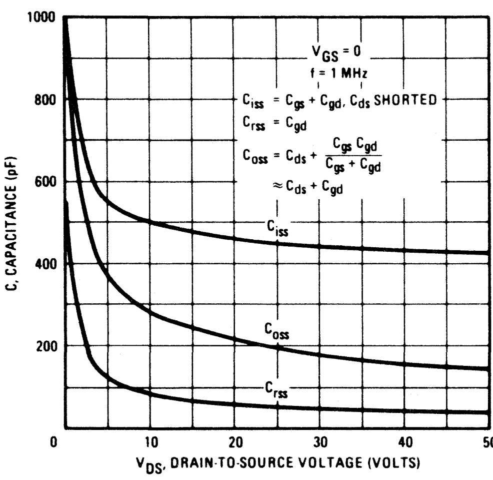


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

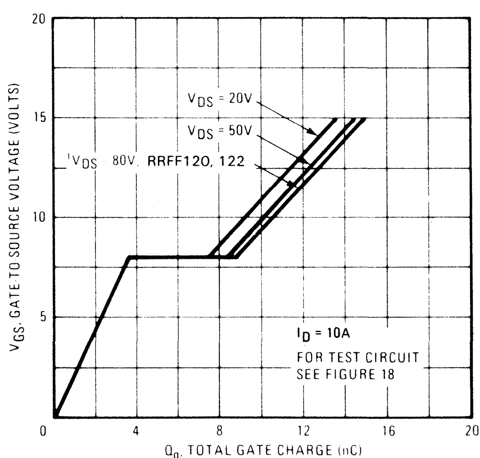


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

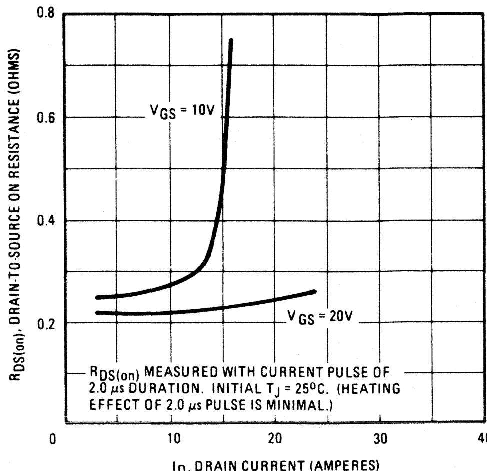


Fig. 12 — Typical On-Resistance Vs. Drain Current

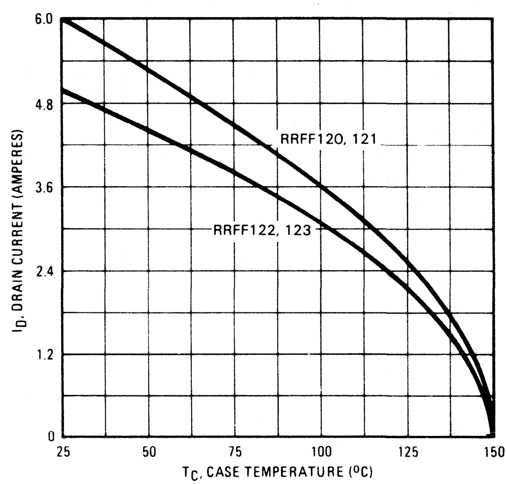


Fig. 13 — Maximum Drain Current Vs. Case Temperature

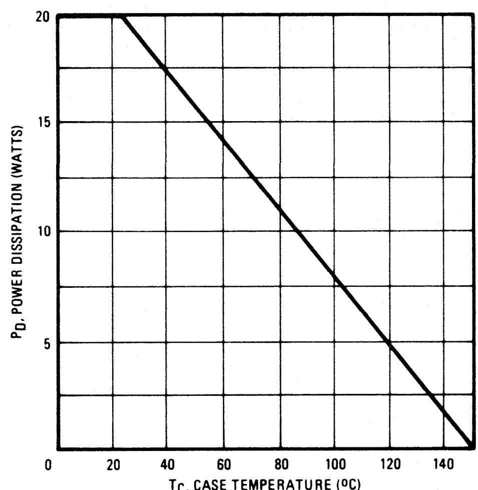


Fig. 14 — Power Vs. Temperature Derating Curve

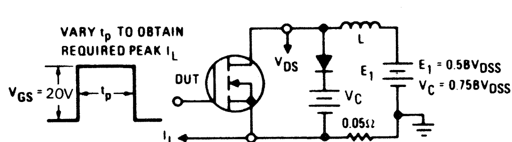


Fig. 15 — Clamped Inductive Test Circuit

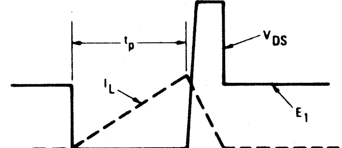


Fig. 16 — Clamped Inductive Waveforms

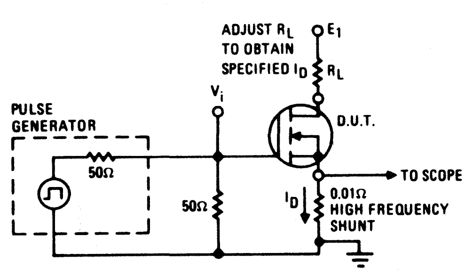


Fig. 17 — Switching Time Test Circuit

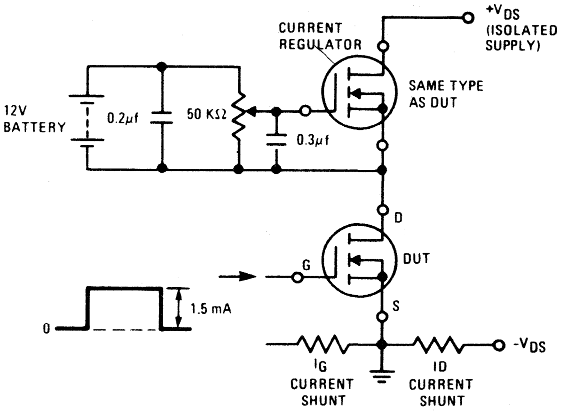


Fig. 18 — Gate Charge Test Circuit

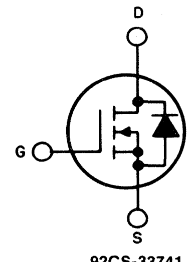
N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

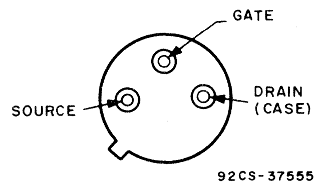
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

The RRFF130, RRFF131, RRFF132 and RRFF133* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.



JEDEC TO-205AF

*These devices are equivalent to International Rectifier Power MOSFETs IRFF130, IRFF131, IRFF132 and IRFF133, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRFF130	RRFF131	RRFF132	RRFF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRFF130 RRFF132	100	–	–	V	V_{GS} = 0V
		RRFF131 RRFF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRFF130 RRFF131	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		RRFF132 RRFF133	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRFF130 RRFF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A
		RRFF132 RRFF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	80	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	80	150	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRFF130 RRFF131	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRFF132 RRFF133	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRFF130 RRFF131	–	–	32	A	
		RRFF132 RRFF133	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	RRFF130 RRFF131	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		RRFF132 RRFF133	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.5	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

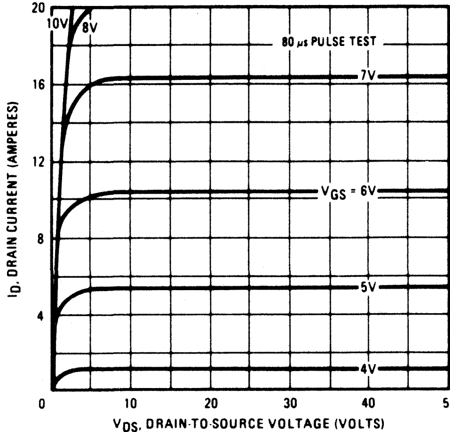


Fig. 1 — Typical Output Characteristics

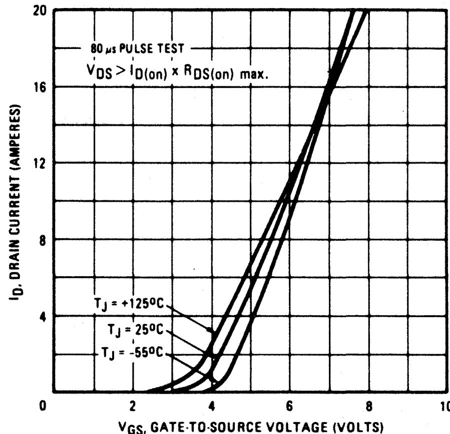


Fig. 2 — Typical Transfer Characteristics

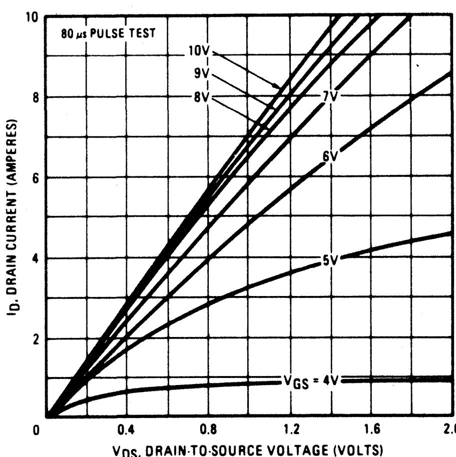


Fig. 3 — Typical Saturation Characteristics

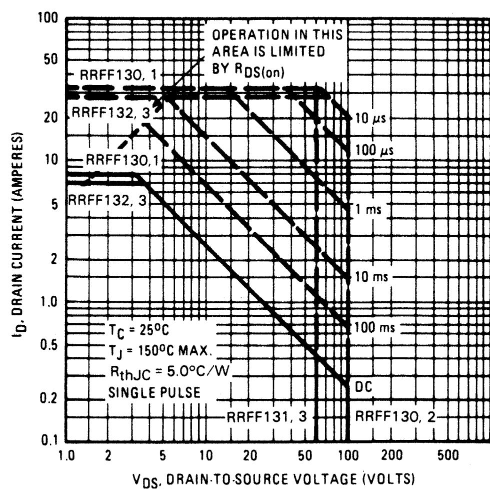


Fig. 4 — Maximum Safe Operating Area

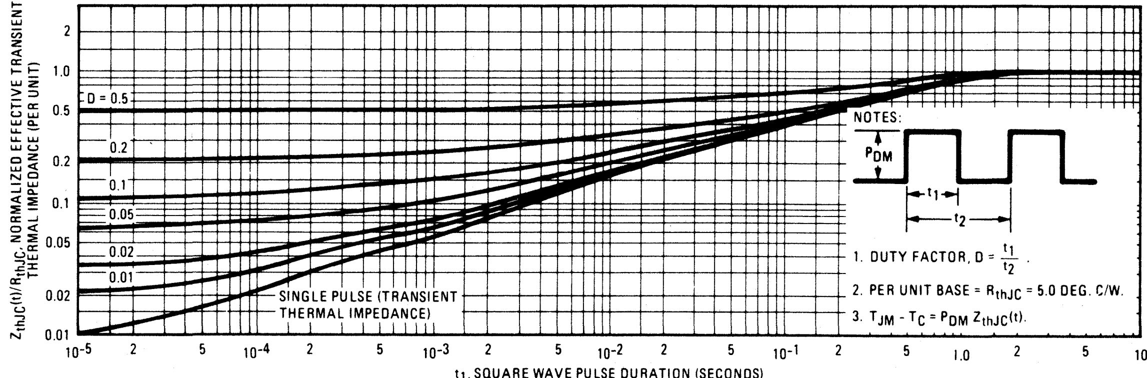


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

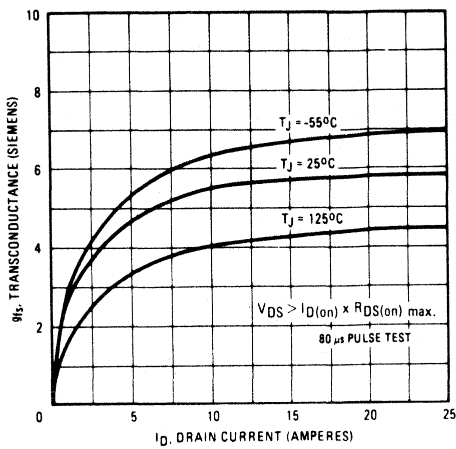


Fig. 6 — Typical Transconductance Vs. Drain Current

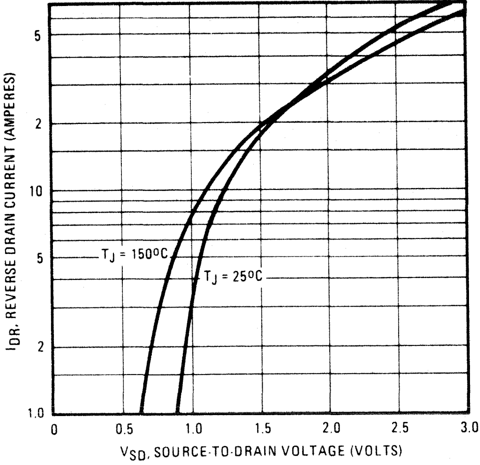


Fig. 7 — Typical Source-Drain Diode Forward Voltage

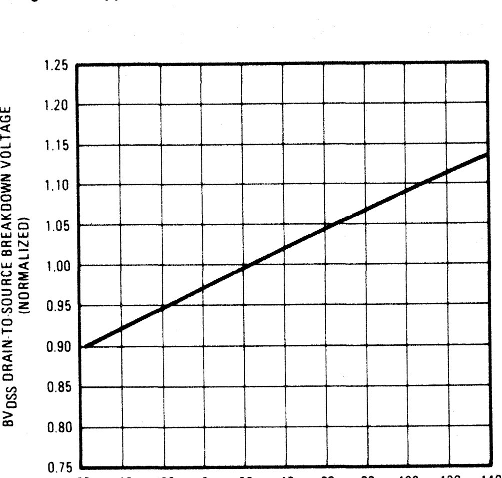


Fig. 8 — Breakdown Voltage Vs. Temperature

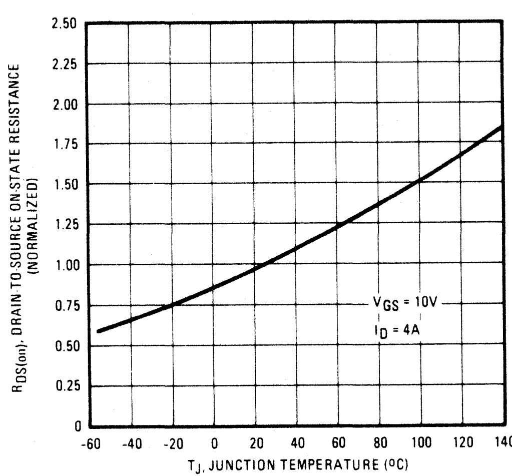


Fig. 9 — Normalized On-Resistance Vs. Temperature

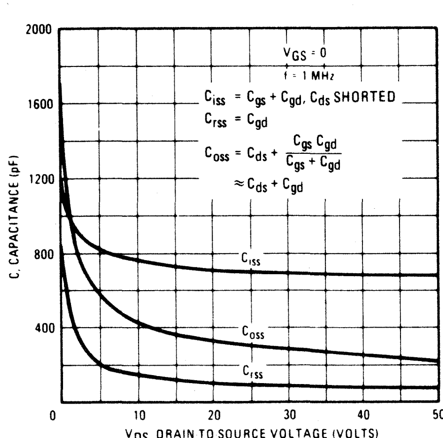


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

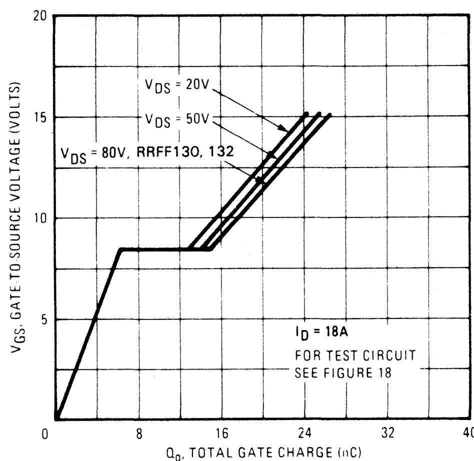


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

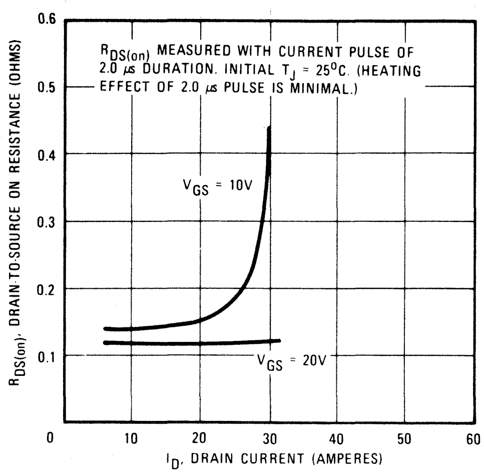


Fig. 12 – Typical On-Resistance Vs. Drain Current

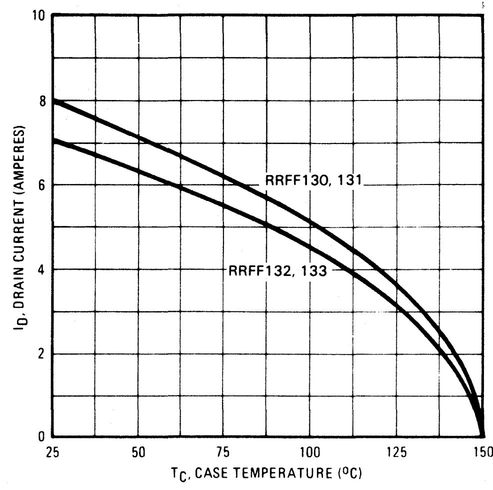


Fig. 13 – Maximum Drain Current Vs. Case Temperature

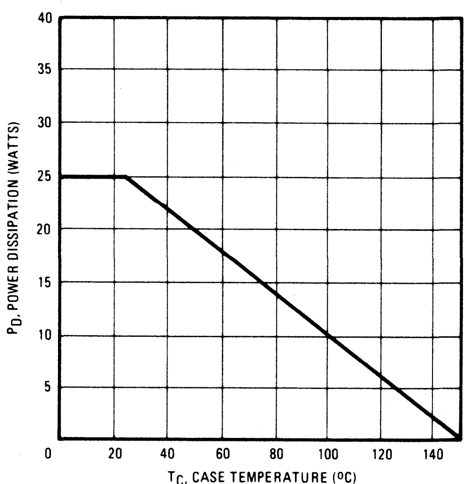


Fig. 14 – Power Vs. Temperature Derating Curve

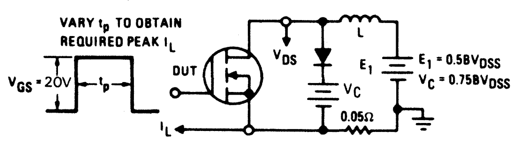


Fig. 15 – Clamped Inductive Test Circuit

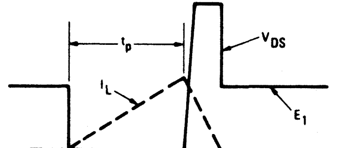


Fig. 16 – Clamped Inductive Waveforms

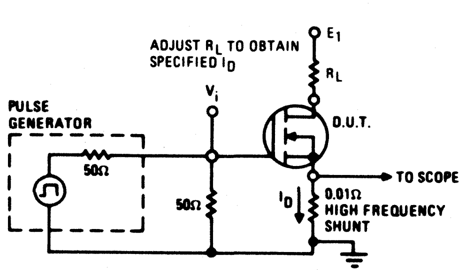


Fig. 17 – Switching Time Test Circuit

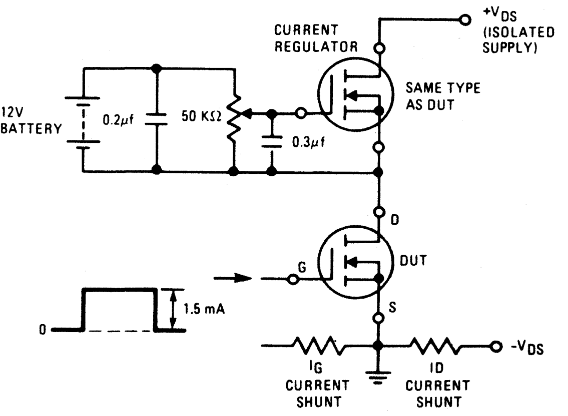


Fig. 18 – Gate Charge Test Circuit

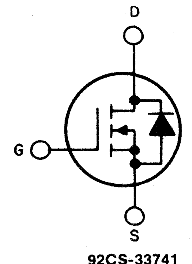
N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

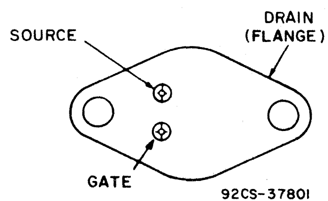


N-CHANNEL ENHANCEMENT MODE

The RRF120, RRF121, RRF122 and RRF123* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

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*These devices are equivalent to International Rectifier Power MOSFETs IRF120, IRF121, IRF122 and IRF123, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF120	RRF121	RRF122	RRF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF120 RRF122	100	–	–	V	V_{GS} = 0V
		RRF121 RRF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF120 RRF121	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF122 RRF123	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF120 RRF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		RRF122 RRF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF120 RRF121	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF122 RRF123	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF120 RRF121	–	–	32	A	
		RRF122 RRF123	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	RRF120 RRF121	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		RRF122 RRF123	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

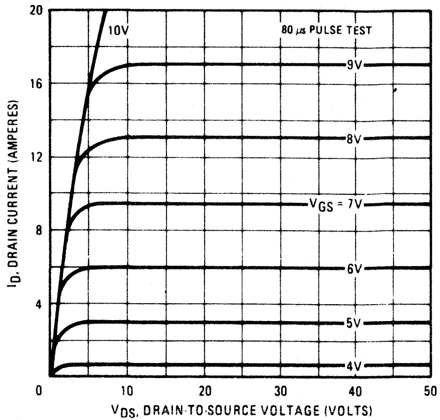


Fig. 1 — Typical Output Characteristics

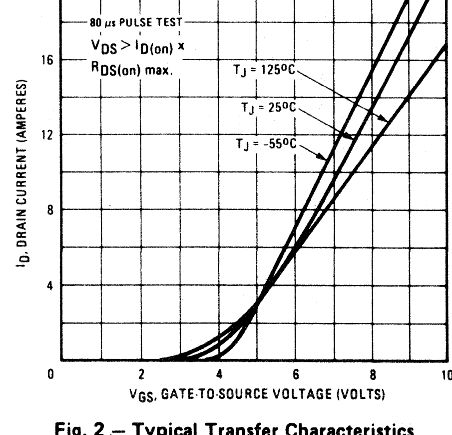


Fig. 2 — Typical Transfer Characteristics

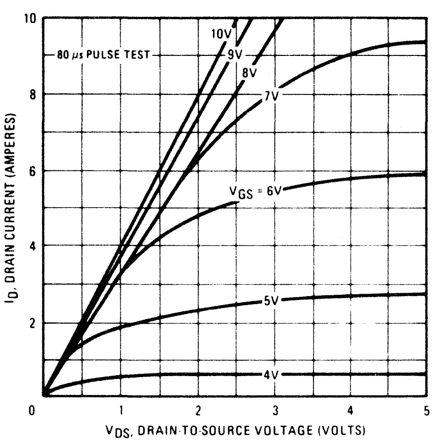


Fig. 3 — Typical Saturation Characteristics

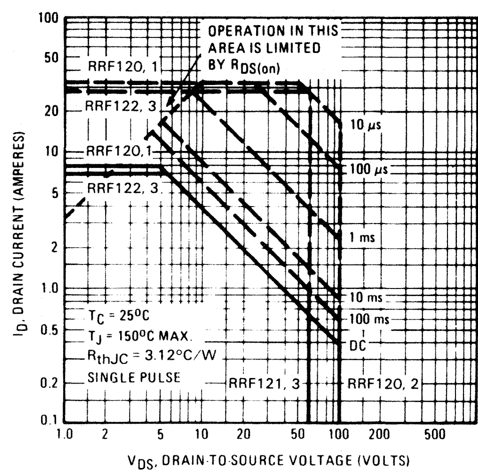


Fig. 4 — Maximum Safe Operating Area

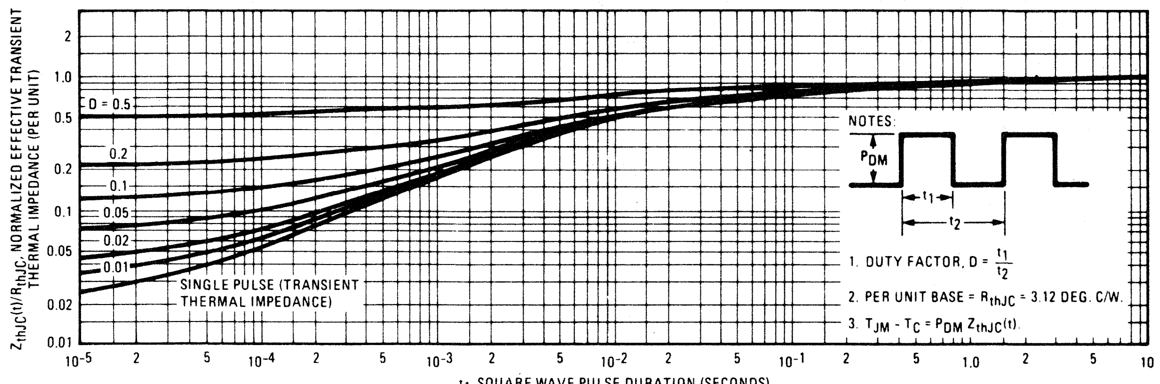


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

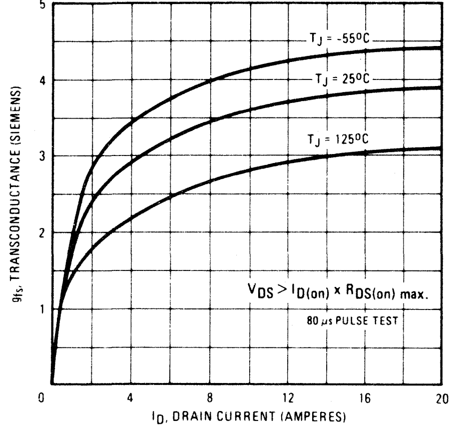


Fig. 6 — Typical Transconductance Vs. Drain Current

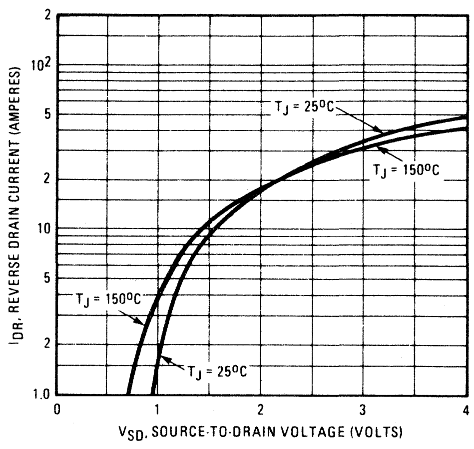


Fig. 7 — Typical Source-Drain Diode Forward Voltage

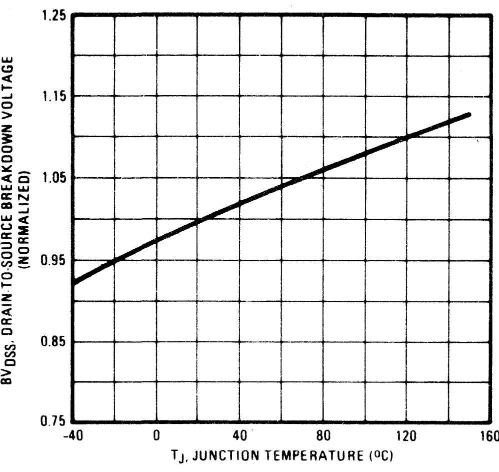


Fig. 8 — Breakdown Voltage Vs. Temperature

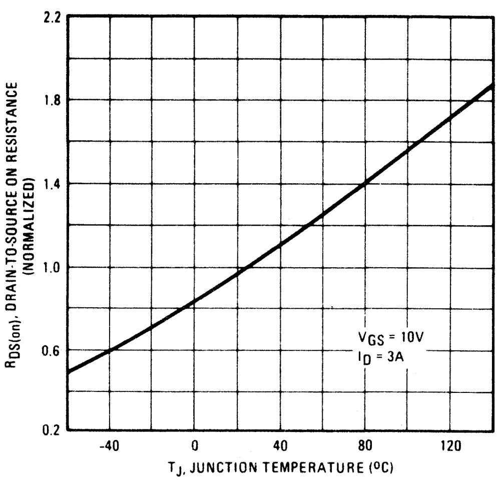


Fig. 9 — Normalized On-Resistance Vs. Temperature

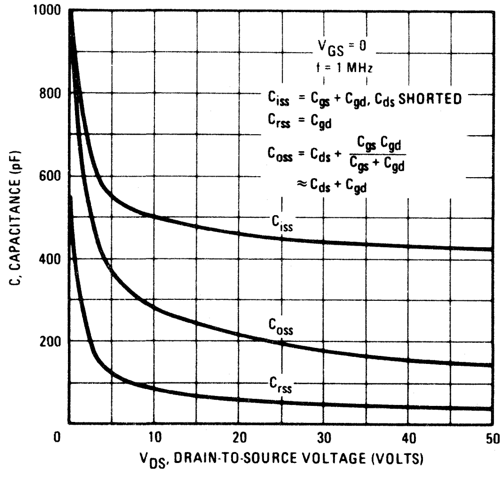


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

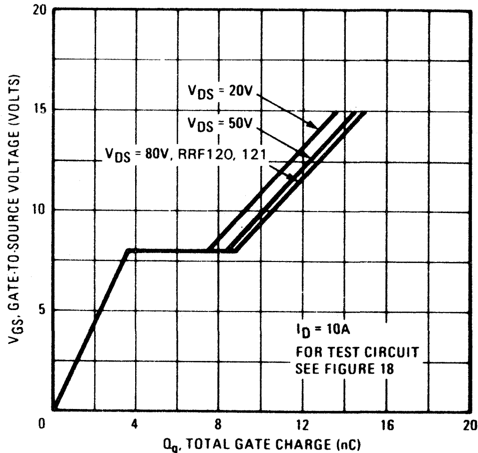


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

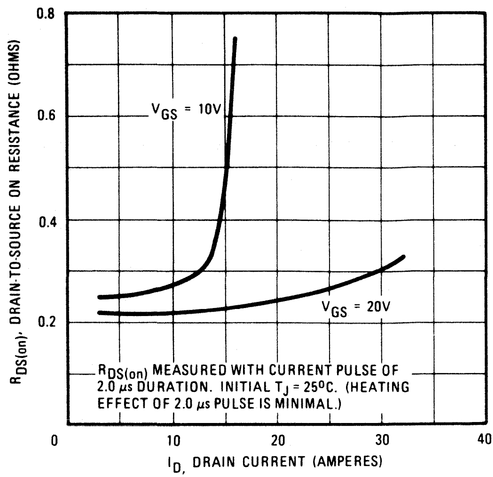


Fig. 12 — Typical On-Resistance Vs. Drain Current

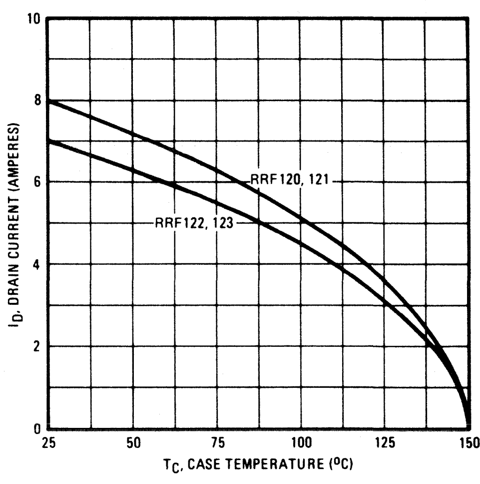


Fig. 13 — Maximum Drain Current Vs. Case Temperature

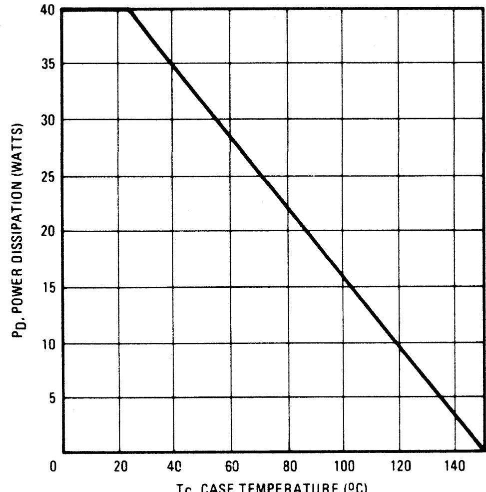


Fig. 14 — Power Vs. Temperature Derating Curve

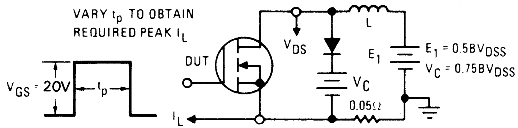


Fig. 15 — Clamped Inductive Test Circuit

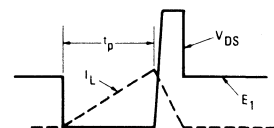


Fig. 16 — Clamped Inductive Waveforms

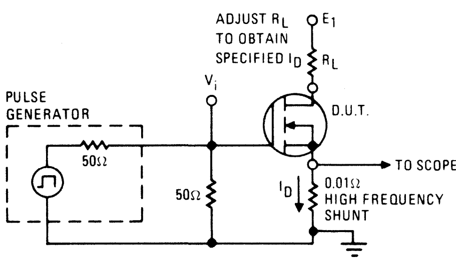


Fig. 17 — Switching Time Test Circuit

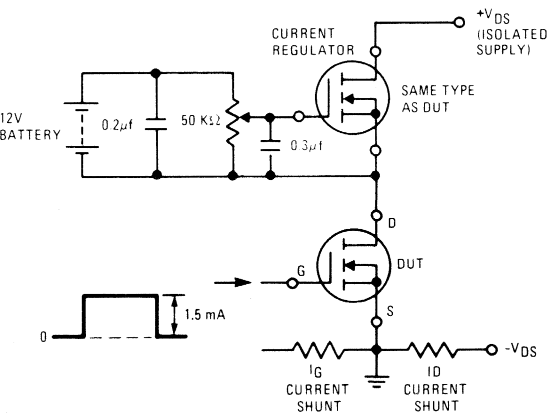


Fig. 18 — Gate Charge Test Circuit

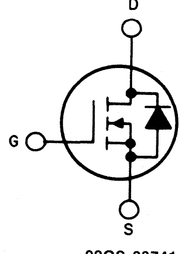
N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

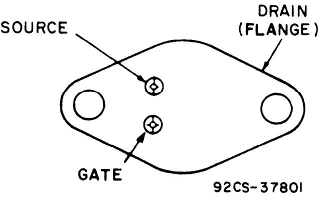
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-204AA

The RRF130, RRF131, RRF132 and RRF133* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF130, IRF131, IRF132 and IRF133, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF130	RRF131	RRF132	RRF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	56	56	48	48	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF130 RRF132	100	—	—	V	V_{GS} = 0V
		RRF131 RRF133	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF130 RRF131	14	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF132 RRF133	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF130 RRF131	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		RRF132 RRF133	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	40	ns	
t_f	Fall Time	ALL	—	—	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF130 RRF131	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF132 RRF133	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF130 RRF131	—	—	56	A	
		RRF132 RRF133	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	RRF130 RRF131	—	—	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		RRF132 RRF133	—	—	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

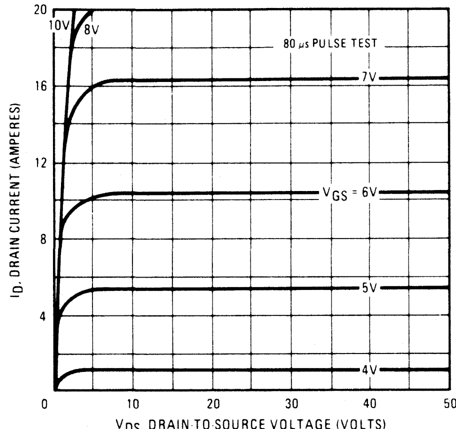


Fig. 1 — Typical Output Characteristics

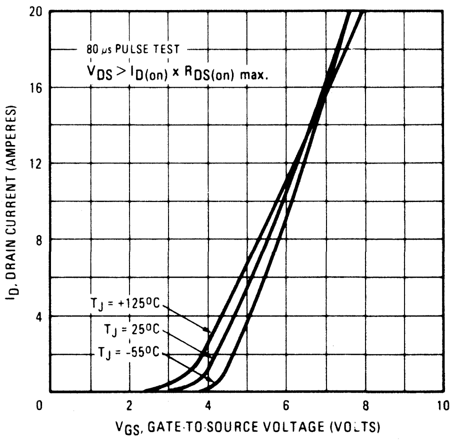


Fig. 2 — Typical Transfer Characteristics

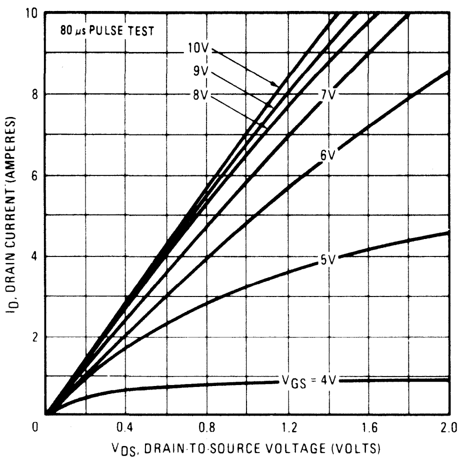


Fig. 3 — Typical Saturation Characteristics

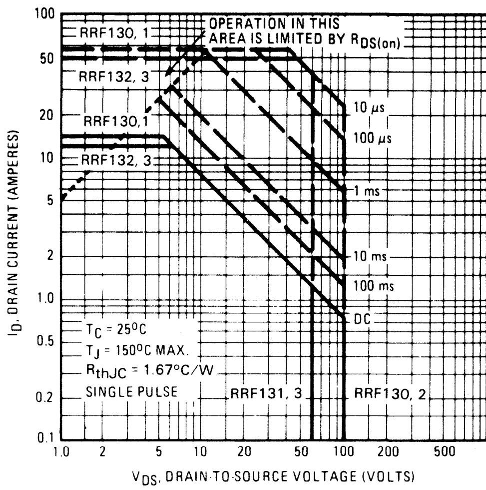


Fig. 4 — Maximum Safe Operating Area

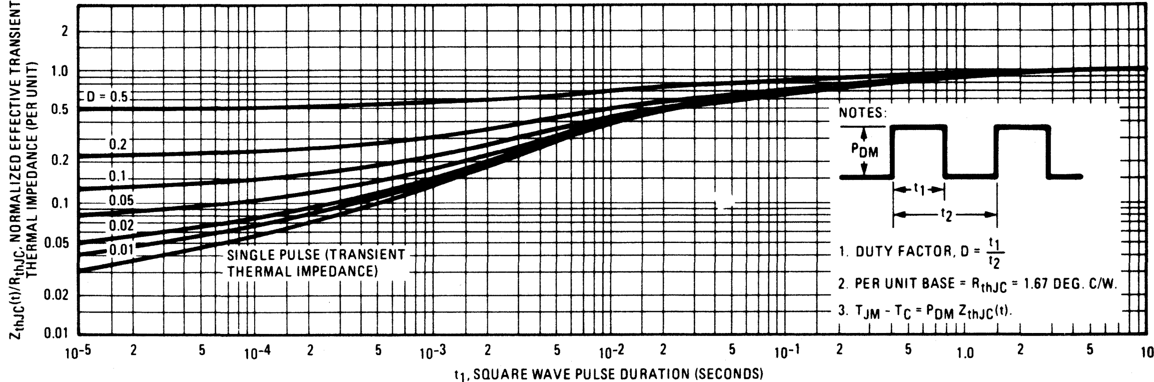


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

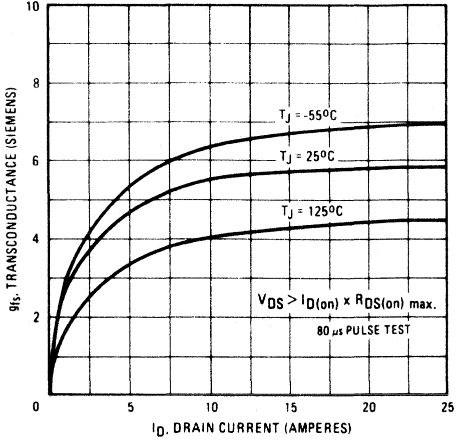


Fig. 6 — Typical Transconductance Vs. Drain Current

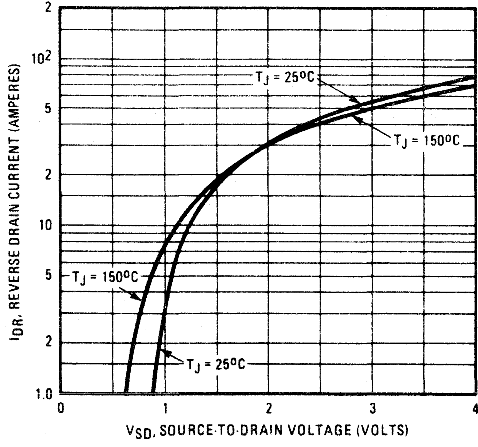


Fig. 7 — Typical Source-Drain Diode Forward Voltage

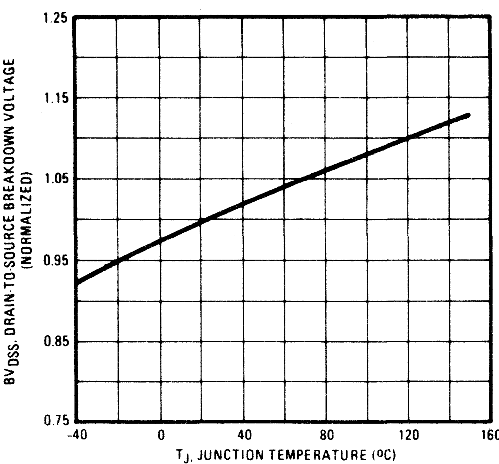


Fig. 8 — Breakdown Voltage Vs. Temperature

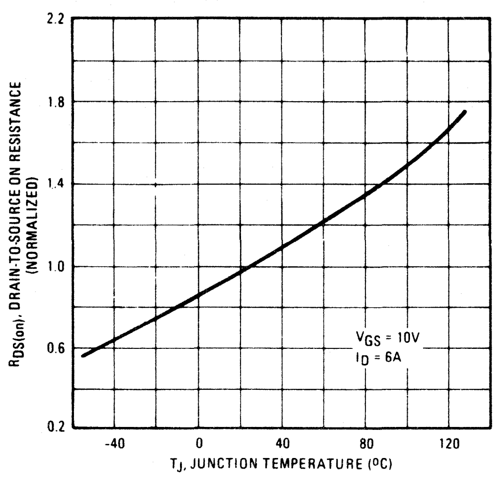


Fig. 9 — Normalized On-Resistance Vs. Temperature

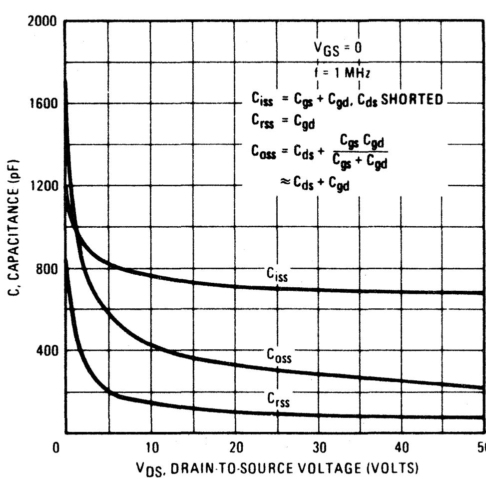


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

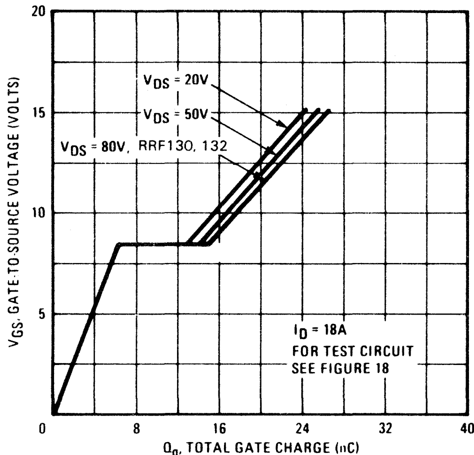


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

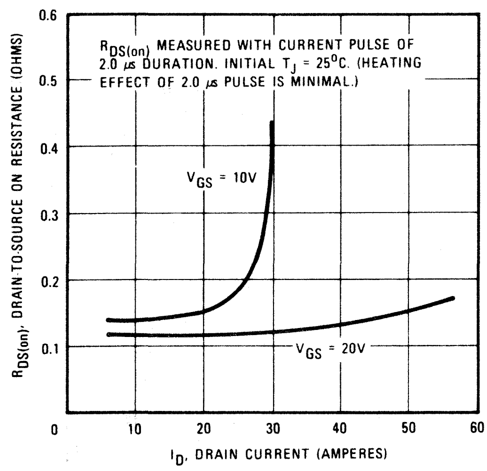


Fig. 12 – Typical On-Resistance Vs. Drain Current

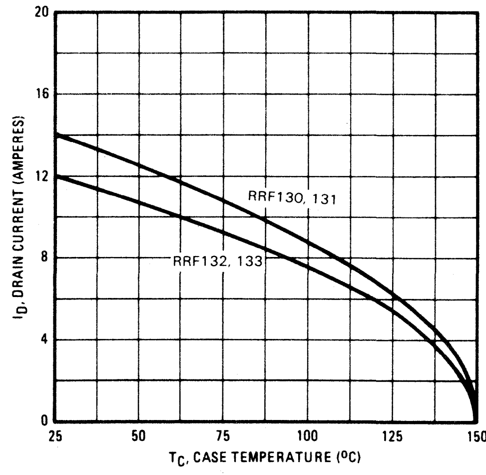


Fig. 13 – Maximum Drain Current Vs. Case Temperature

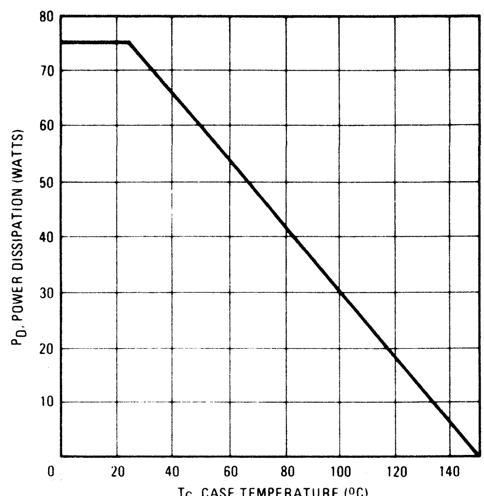


Fig. 14 – Power Vs. Temperature Derating Curve

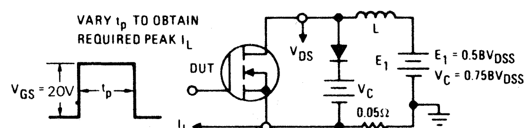


Fig. 15 – Clamped Inductive Test Circuit

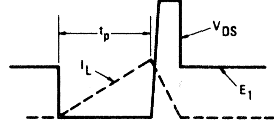


Fig. 16 – Clamped Inductive Waveforms

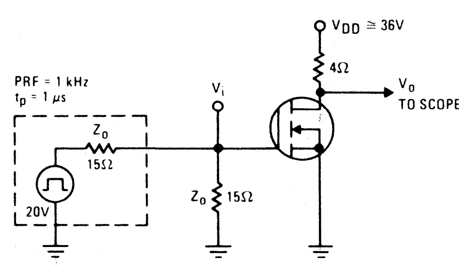


Fig. 17 – Switching Time Test Circuit

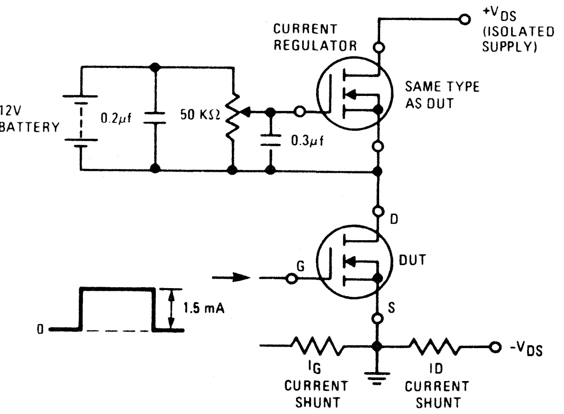


Fig. 18 – Gate Charge Test Circuit

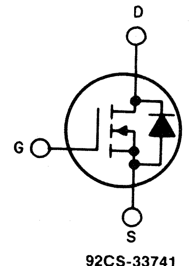
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

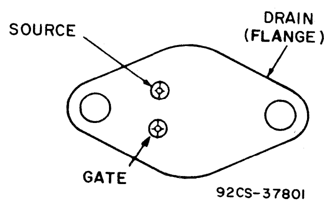


N-CHANNEL ENHANCEMENT MODE

The RRF220, RRF221, RRF222 and RRF223* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

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*These devices are equivalent to International Rectifier Power MOSFETs IRF220, IRF221, IRF222 and IRF223, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF220	RRF221	RRF222	RRF223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 20	20	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-50 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

RRF220, RRF221, RRF222, RRF223

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF220 RRF222	200	–	–	V	V_{GS} = 0V
		RRF221 RRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF220 RRF221	5.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF222 RRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF220 RRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		RRF222 RRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF220 RRF221	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF222 RRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF220 RRF221	–	–	20	A	
		RRF222 RRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	RRF220 RRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		RRF222 RRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

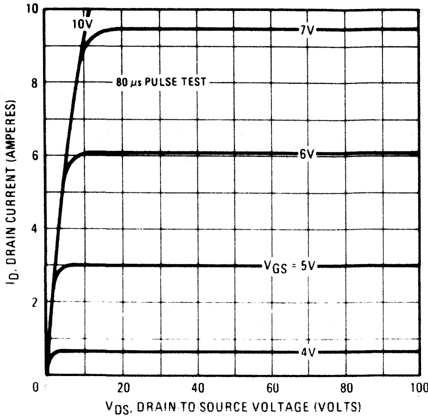


Fig. 1 — Typical Output Characteristics

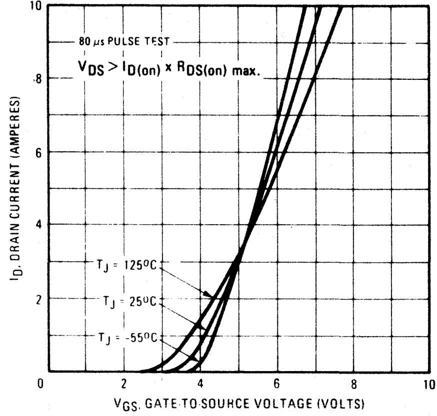


Fig. 2 — Typical Transfer Characteristics

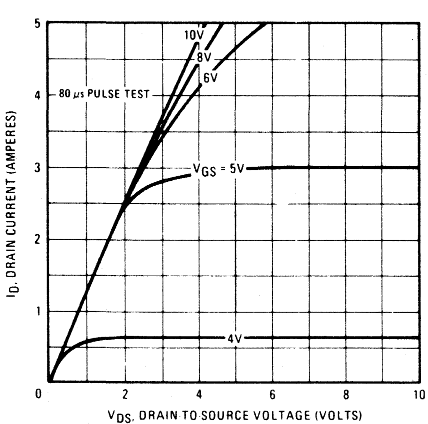


Fig. 3 — Typical Saturation Characteristics

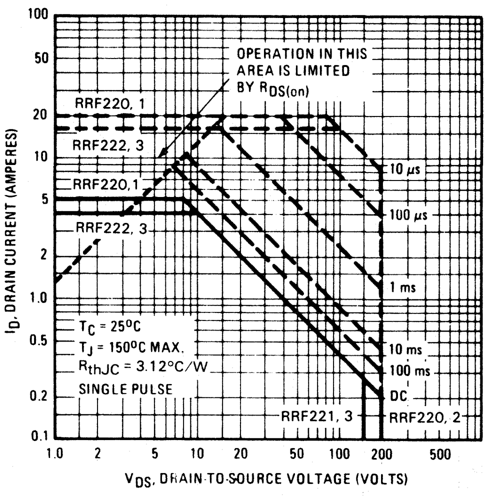


Fig. 4 — Maximum Safe Operating Area

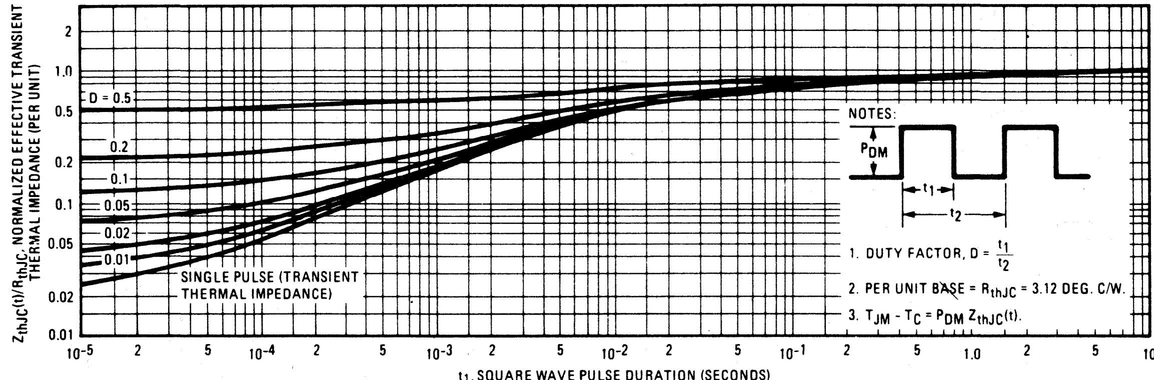


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

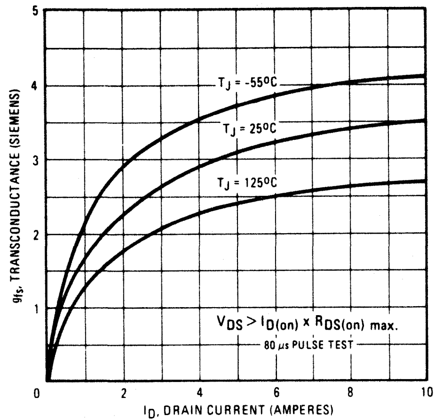


Fig. 6 — Typical Transconductance Vs. Drain Current

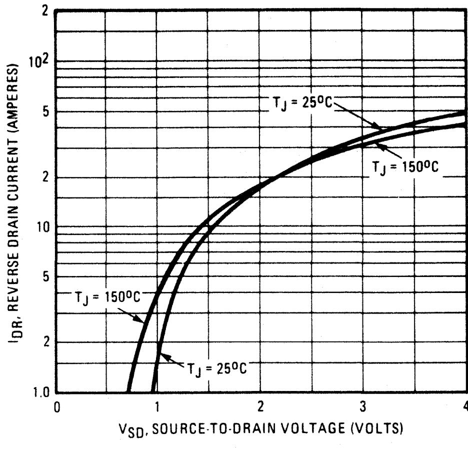


Fig. 7 — Typical Source-Drain Diode Forward Voltage

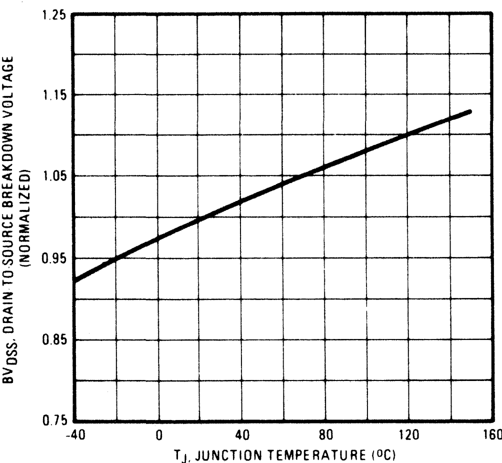


Fig. 8 — Breakdown Voltage Vs. Temperature

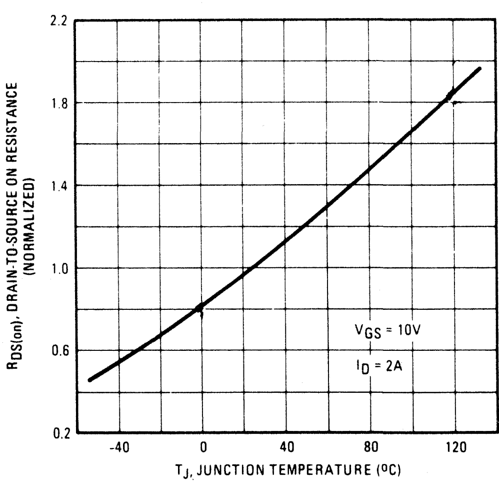


Fig. 9 — Normalized On-Resistance Vs. Temperature

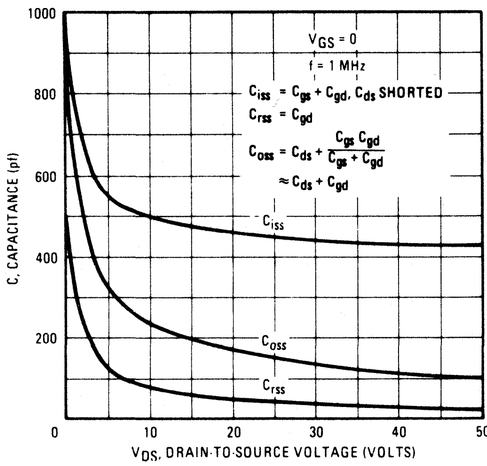


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

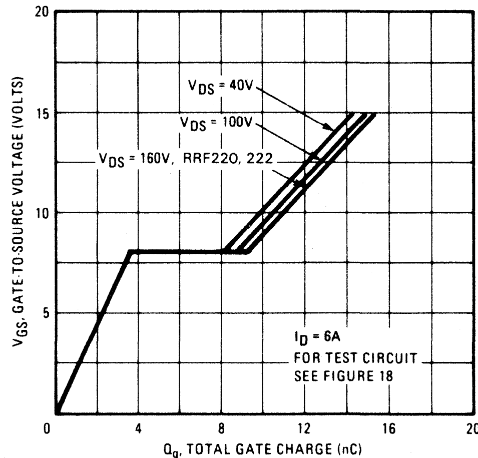


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

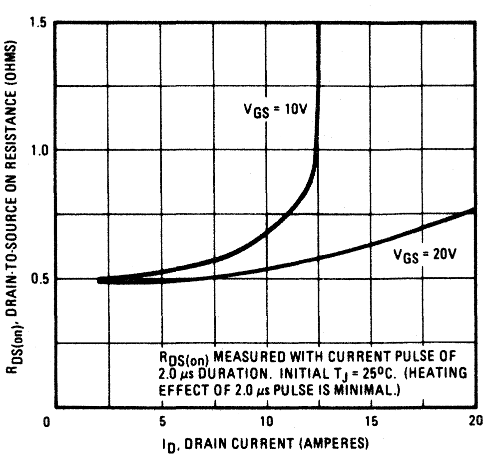


Fig. 12 – Typical On-Resistance Vs. Drain Current

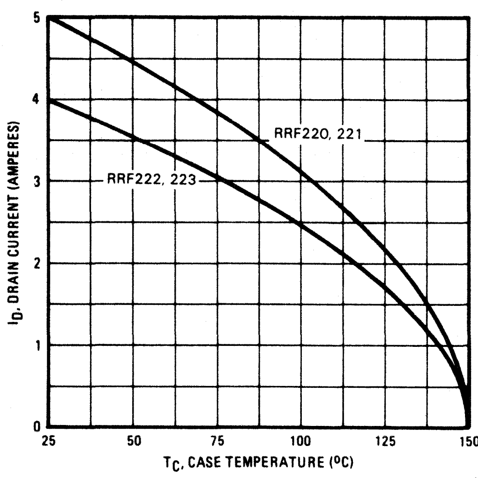


Fig. 13 – Maximum Drain Current Vs. Case Temperature

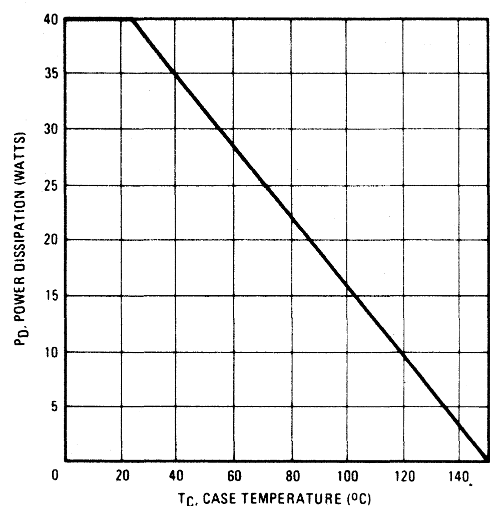


Fig. 14 – Power Vs. Temperature Derating Curve

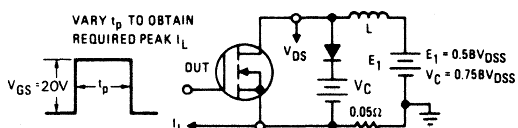


Fig. 15 – Clamped Inductive Test Circuit

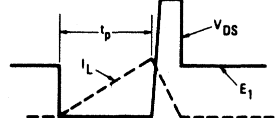


Fig. 16 – Clamped Inductive Waveforms

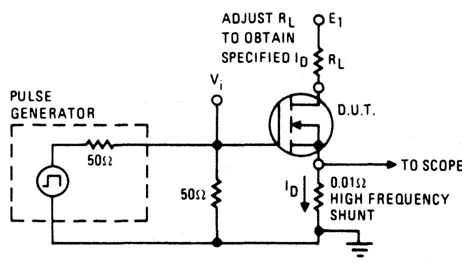


Fig. 17 – Switching Time Test Circuit

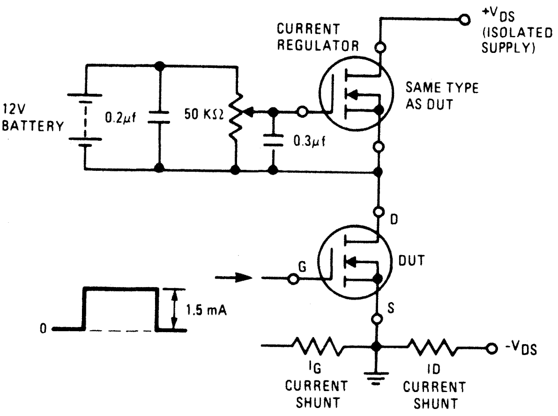


Fig. 18 – Gate Charge Test Circuit

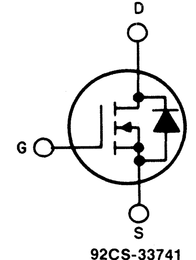
N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



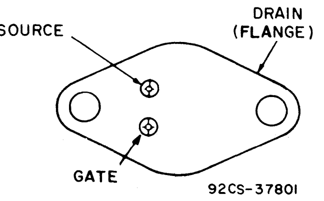
N-CHANNEL ENHANCEMENT MODE

The RRF230, RRF231, RRF232 and RRF233* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF230, IRF231, IRF232 and IRF233, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

	Parameter	RRF230	RRF231	RRF232	RRF233	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 36	36	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF230 RRF232	200	–	–	V	V_{GS} = 0V
		RRF231 RRF233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF230 RRF231	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		RRF232 RRF233	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF230 RRF231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		RRF232 RRF233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF230 RRF231	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF232 RRF233	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF230 RRF231	–	–	36	A	
		RRF232 RRF233	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	RRF230 RRF231	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		RRF232 RRF233	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

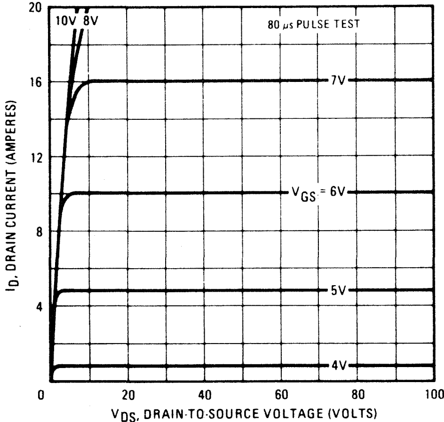


Fig. 1 — Typical Output Characteristics

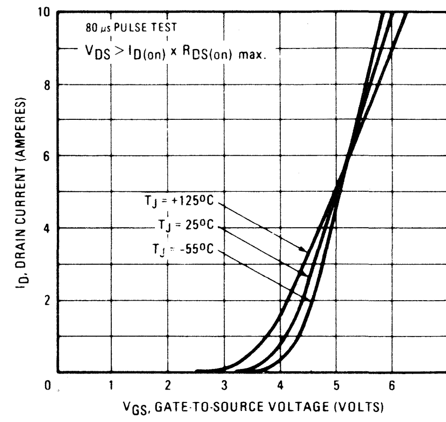


Fig. 2 — Typical Transfer Characteristics

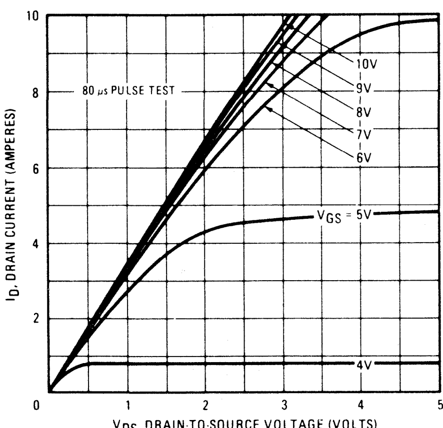


Fig. 3 — Typical Saturation Characteristics

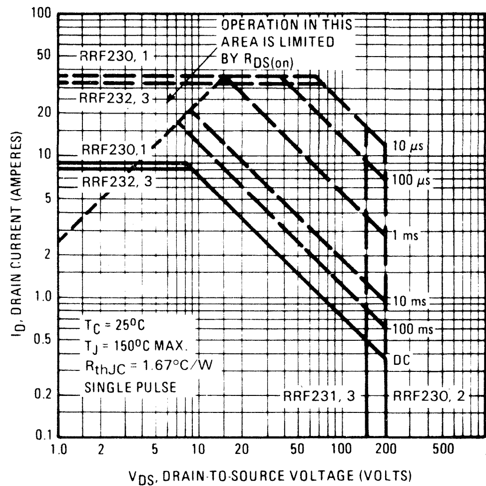


Fig. 4 — Maximum Safe Operating Area

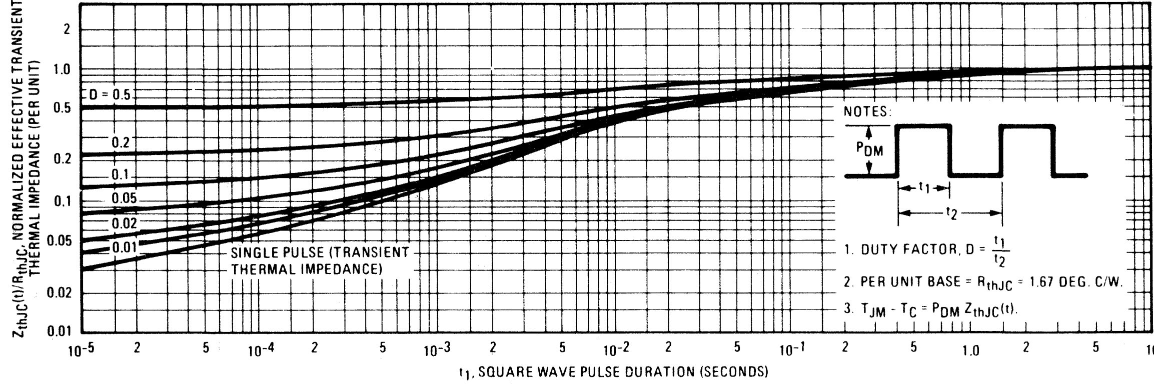


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

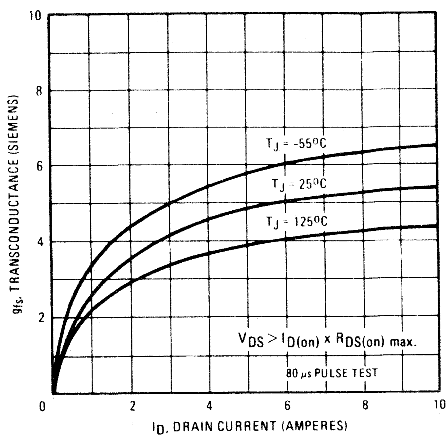


Fig. 6 — Typical Transconductance Vs. Drain Current

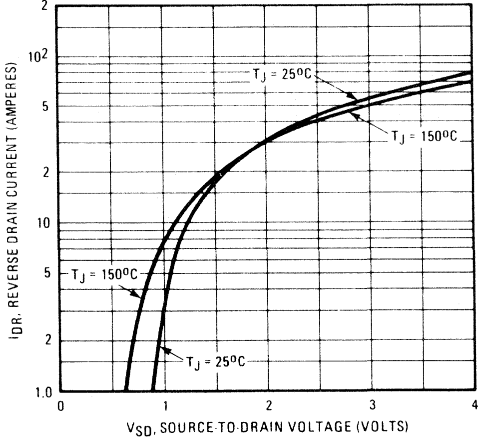


Fig. 7 — Typical Source-Drain Diode Forward Voltage

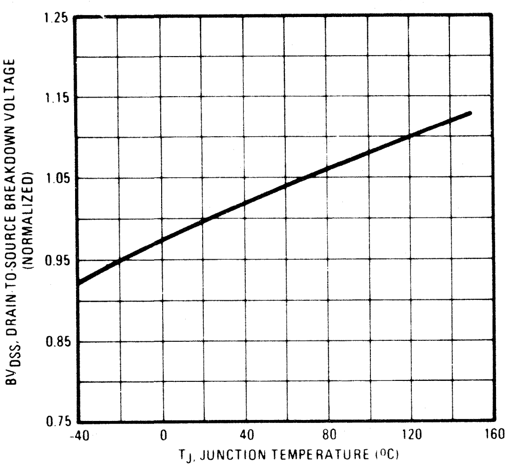


Fig. 8 — Breakdown Voltage Vs. Temperature

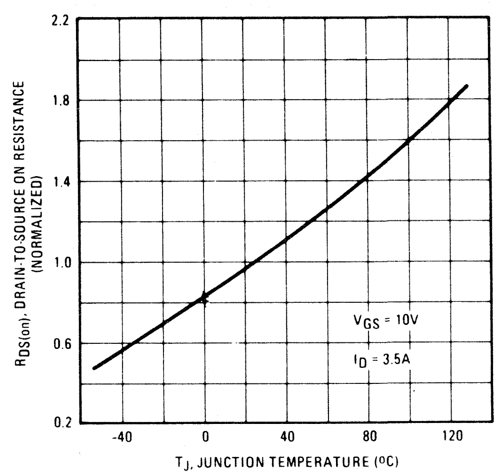


Fig. 9 — Normalized On-Resistance Vs. Temperature

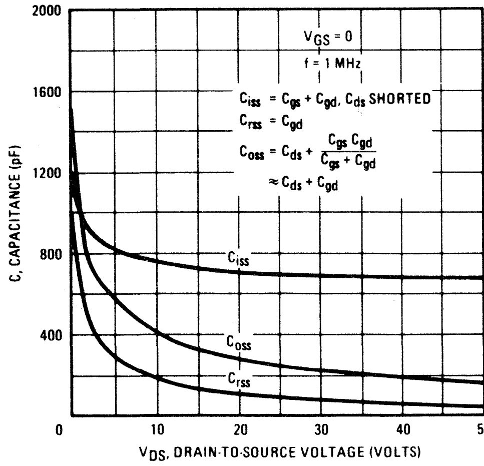


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

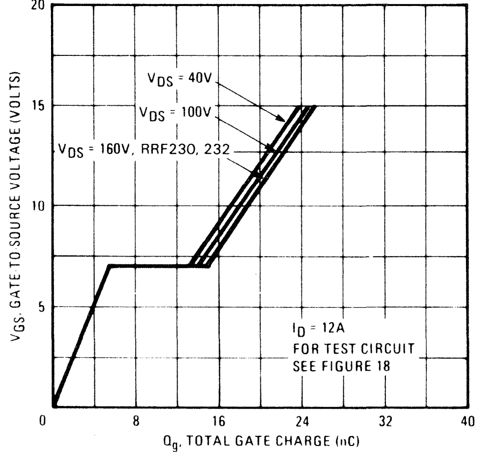


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

RRF230, RRF231, RRF232, RRF233

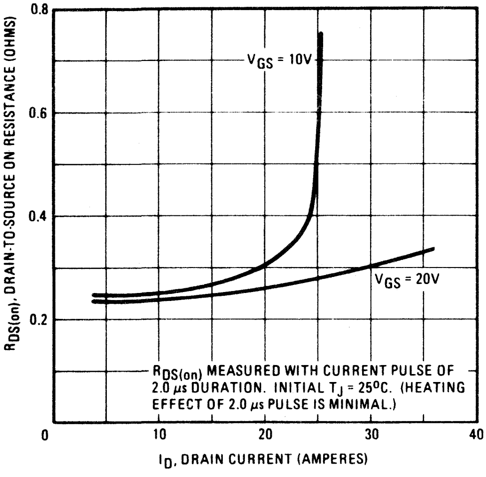


Fig. 12 – Typical On-Resistance Vs. Drain Current

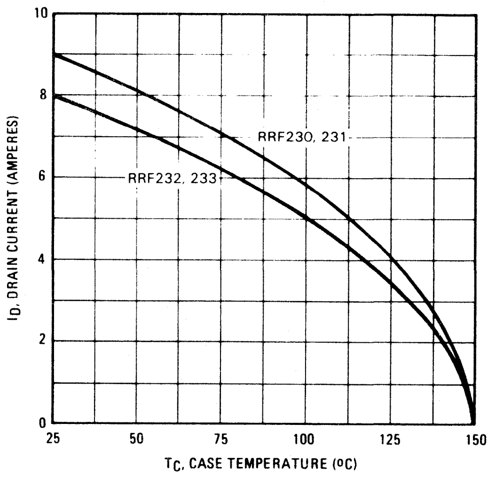


Fig. 13 – Maximum Drain Current Vs. Case Temperature

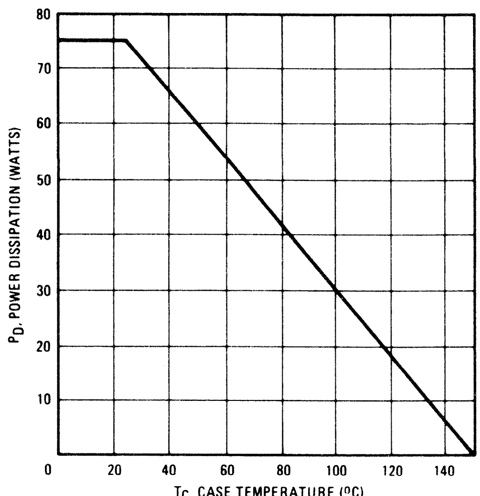


Fig. 14 – Power Vs. Temperature Derating Curve

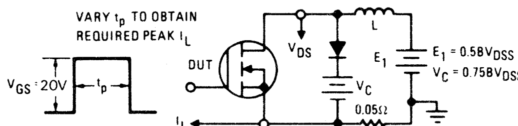


Fig. 15 – Clamped Inductive Test Circuit

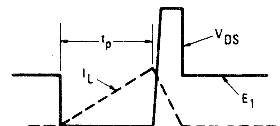


Fig. 16 – Clamped Inductive Waveforms

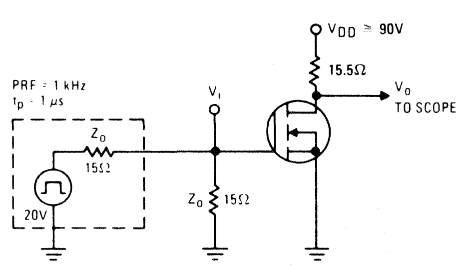


Fig. 17 – Switching Time Test Circuit

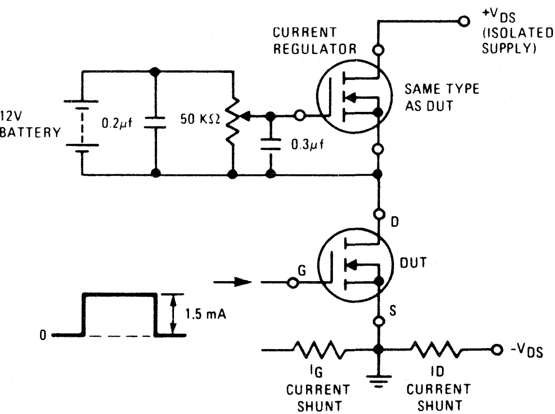


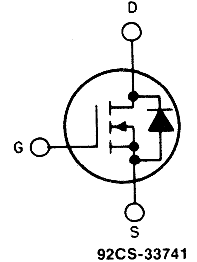
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

16A and 18A, 150V

$r_{DS}(on)$ = 0.18 Ω and 0.22 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

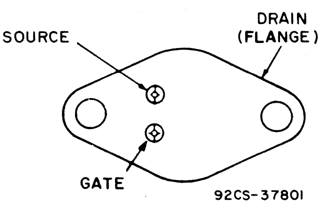


N-CHANNEL ENHANCEMENT MODE

The RRF241 and RRF243* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

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*These devices are equivalent to International Rectifier Power MOSFETs IRF241 and IRF243, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF241	RRF243	Units
V_{DS}	Drain - Source Voltage ①	150	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	150	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	10	A
I_{DM}	Pulsed Drain Current ③	72	64	A
V_{GS}	Gate - Source Voltage	± 20		V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)		W
	Linear Derating Factor	1.0 (See Fig. 14)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 72 | 72	64 | 64	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

RRF241, RRF243

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF241 RRF243	150	–	–	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF241	18	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF243	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF241	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		RRF243	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF241	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF243	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF241	–	–	72	A	
		RRF243	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	RRF241	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		RRF243	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

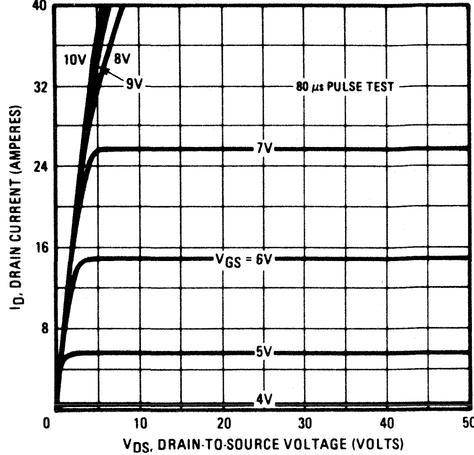


Fig. 1 — Typical Output Characteristics

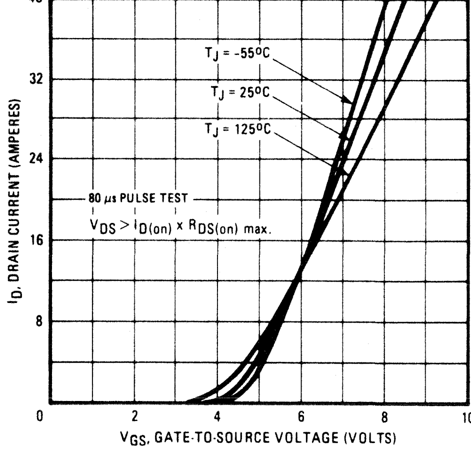


Fig. 2 — Typical Transfer Characteristics

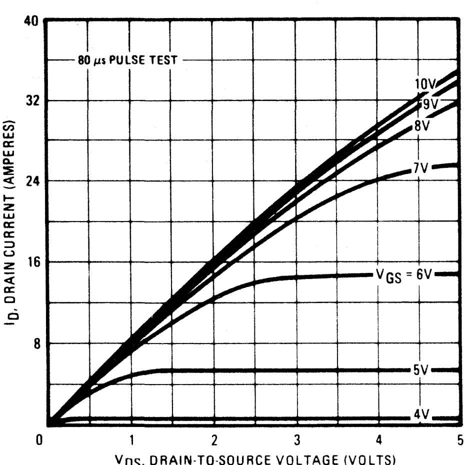


Fig. 3 — Typical Saturation Characteristics

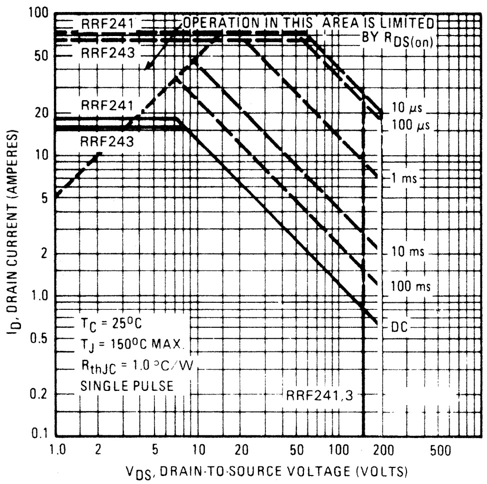


Fig. 4 — Maximum Safe Operating Area

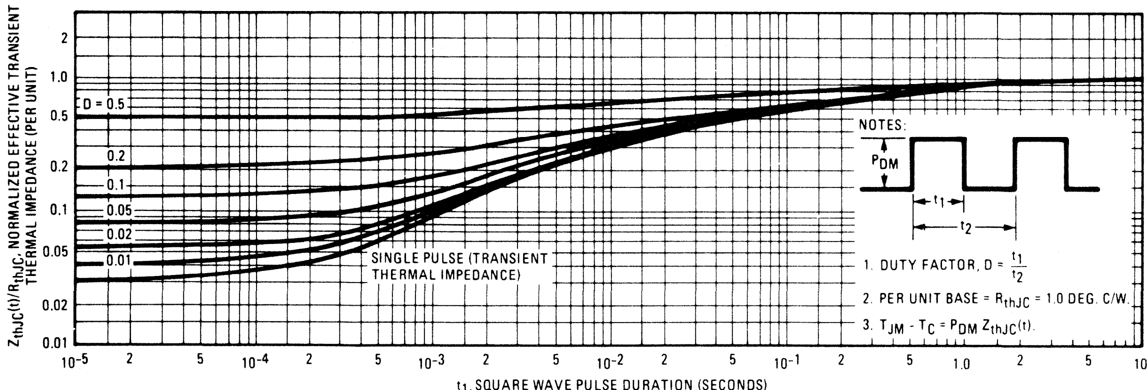


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

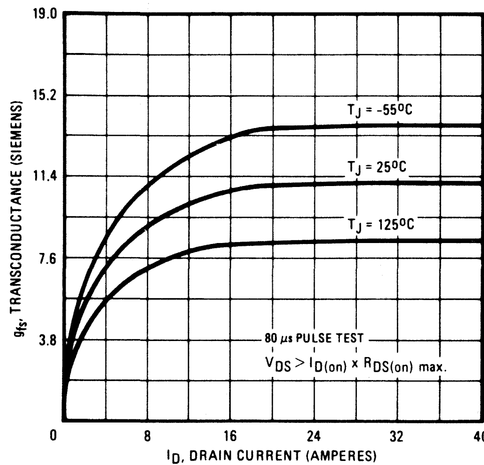


Fig. 6 — Typical Transconductance Vs. Drain Current

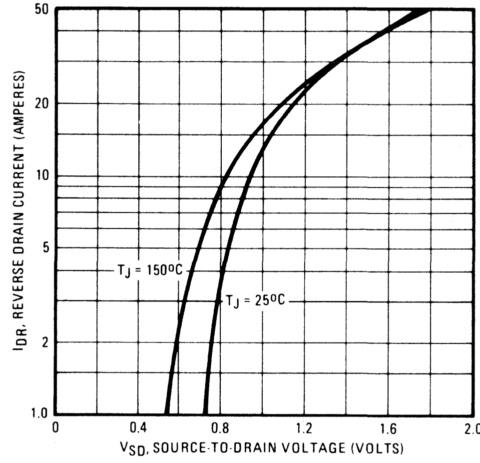


Fig. 7 — Typical Source-Drain Diode Forward Voltage

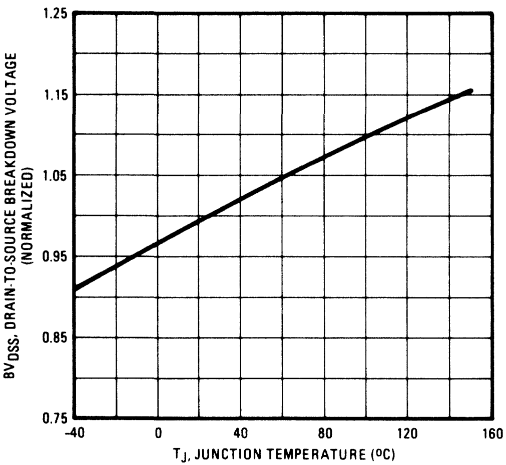


Fig. 8 — Breakdown Voltage Vs. Temperature

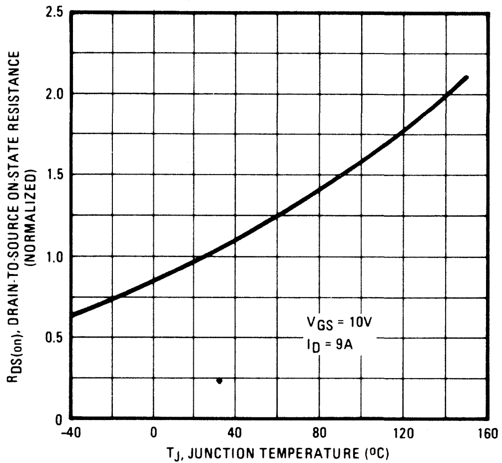


Fig. 9 — Normalized On-Resistance Vs. Temperature

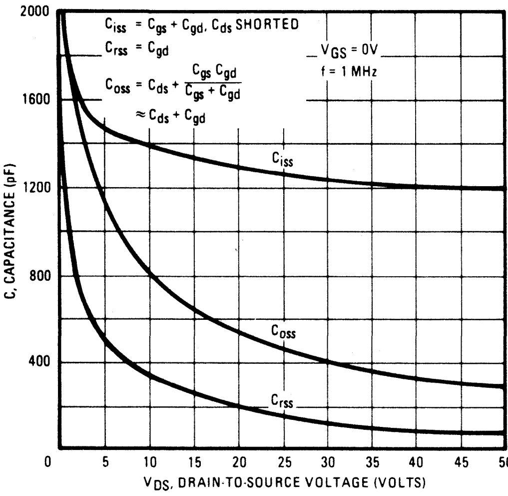


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

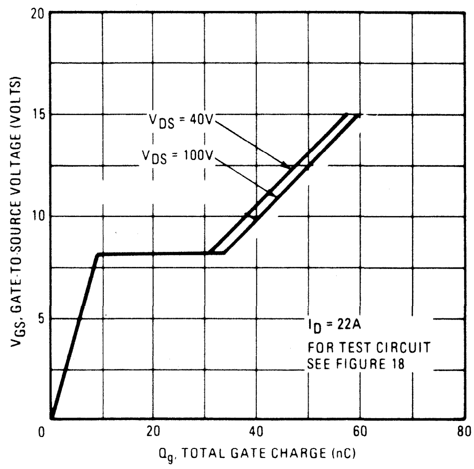


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

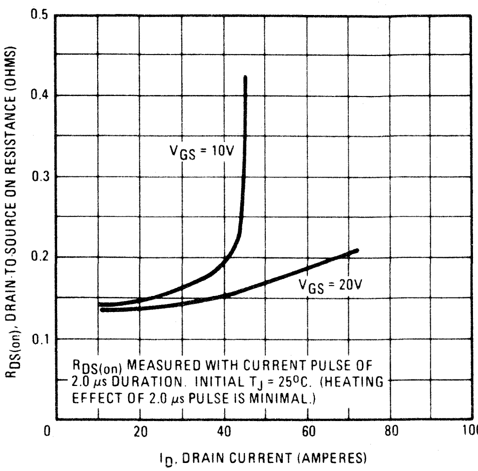


Fig. 12 – Typical On-Resistance Vs. Drain Current

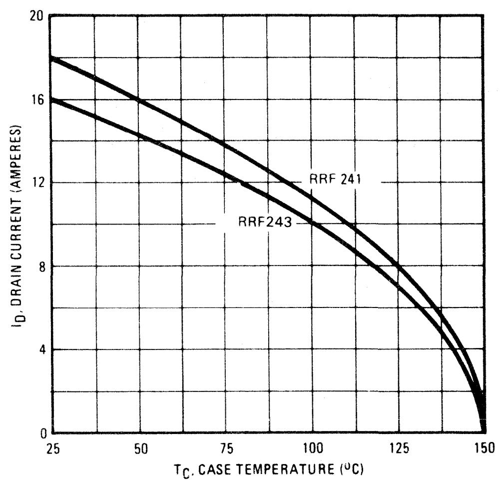


Fig. 13 – Maximum Drain Current Vs. Case Temperature

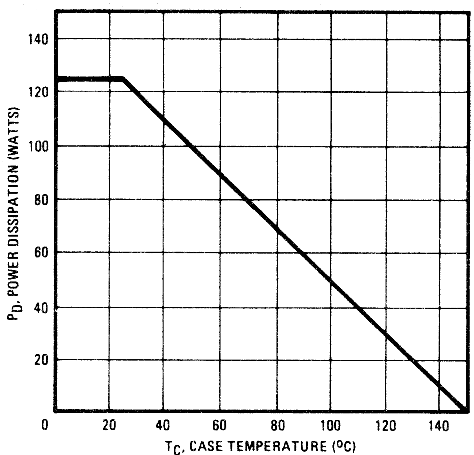


Fig. 14 – Power Vs. Temperature Derating Curve

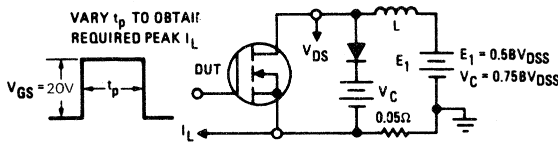


Fig. 15 – Clamped Inductive Test Circuit

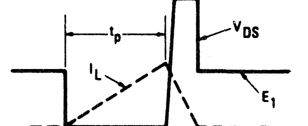


Fig. 16 – Clamped Inductive Waveforms

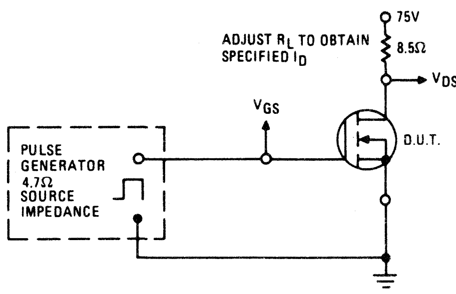


Fig. 17 – Switching Time Test Circuit

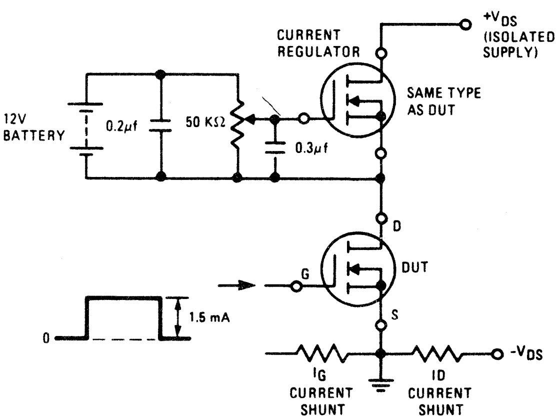


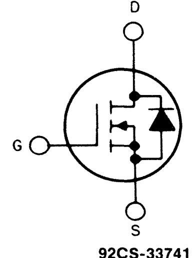
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

25A and 30A, 120V - 150V

$r_{DS}(on)$ = 0.085 Ω and 0.120 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

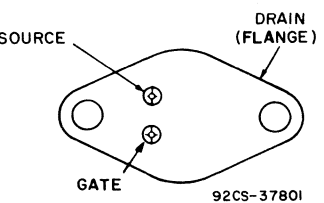
N-CHANNEL ENHANCEMENT MODE

The RRF251 and RRF253* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AE steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF251 and IRF253, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AE

Absolute Maximum Ratings

	Parameter	RRF251	RRF253	Units
V_{DS}	Drain - Source Voltage ①	150	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	150	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	16	A
I_{DM}	Pulsed Drain Current ③	120	100	A
V_{GS}	Gate - Source Voltage	± 20		V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)		W
	Linear Derating Factor	1.2 (See Fig. 14)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 120 120	100 100	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF251 RRF253	150	–	–	V	V_{GS} = 0V I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF251	30	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF253	25	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF251	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		RRF253	–	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 16A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	800	1200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	300	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	37	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF251	–	–	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF253	–	–	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF251	–	–	120	A	
		RRF253	–	–	100	A	
V_{SD}	Diode Forward Voltage ②	RRF251	–	–	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		RRF253	–	–	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	750	–	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.7	–	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

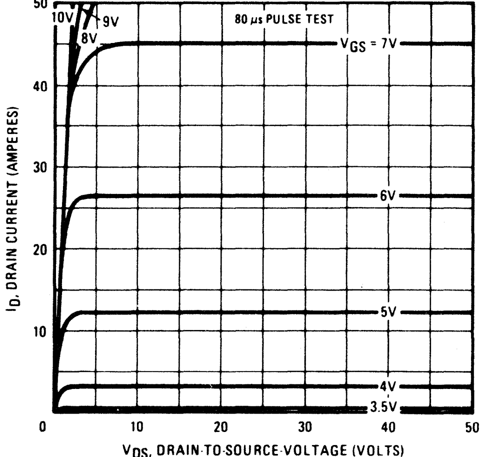


Fig. 1 – Typical Output Characteristics

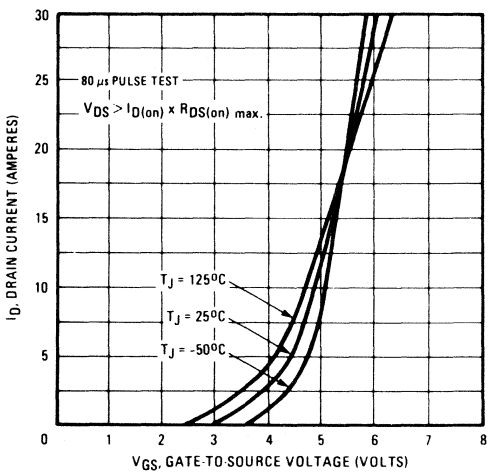


Fig. 2 – Typical Transfer Characteristics

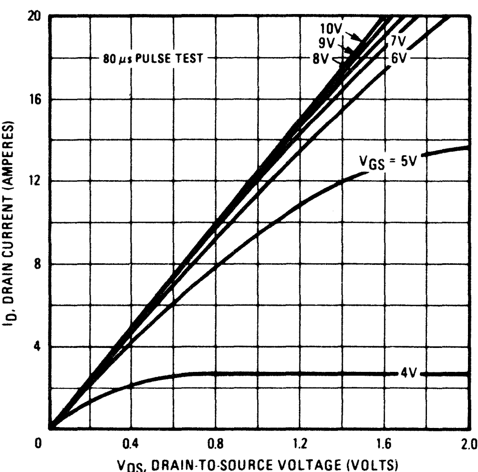


Fig. 3 – Typical Saturation Characteristics

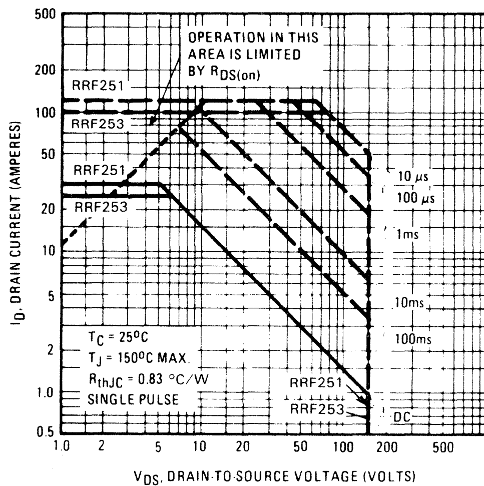


Fig. 4 – Maximum Safe Operating Area

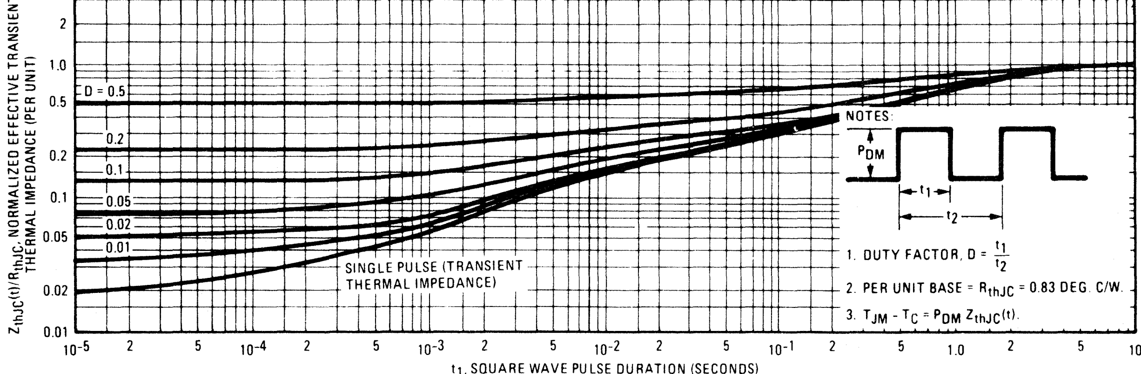


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

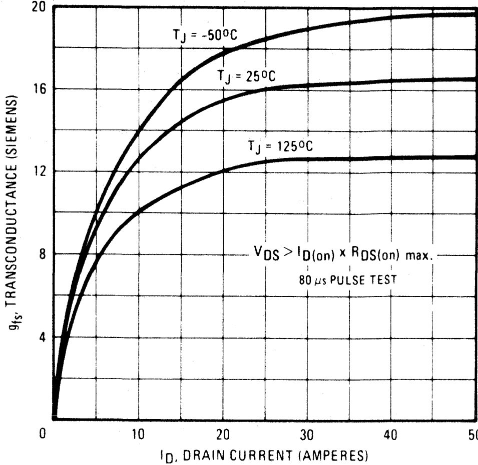


Fig. 6 — Typical Transconductance Vs. Drain Current

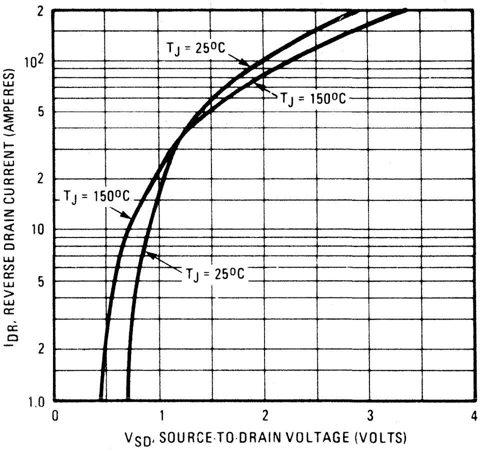


Fig. 7 — Typical Source-Drain Diode Forward Voltage

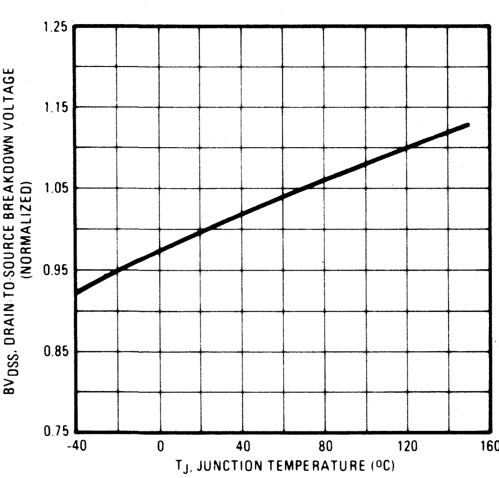


Fig. 8 — Breakdown Voltage Vs. Temperature

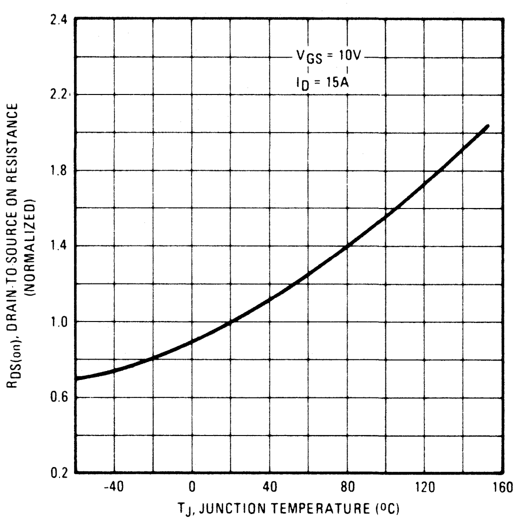


Fig. 9 — Normalized On-Resistance Vs. Temperature

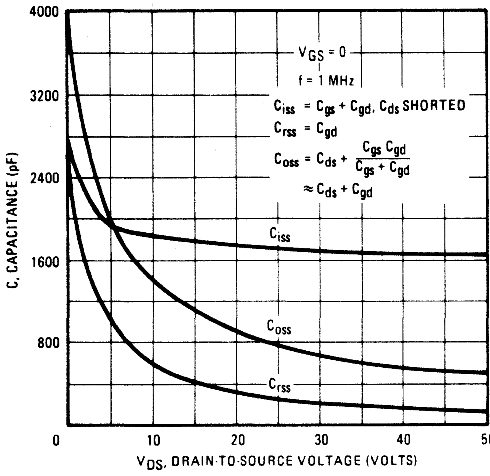


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

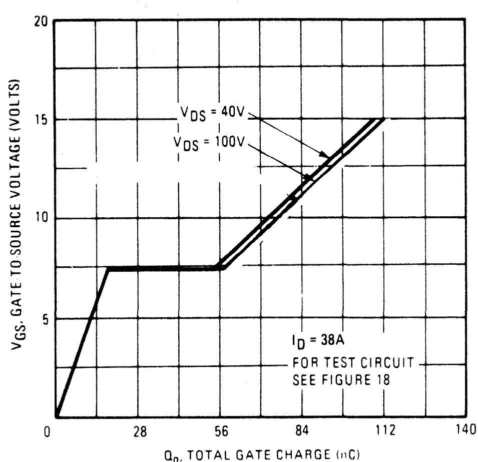


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

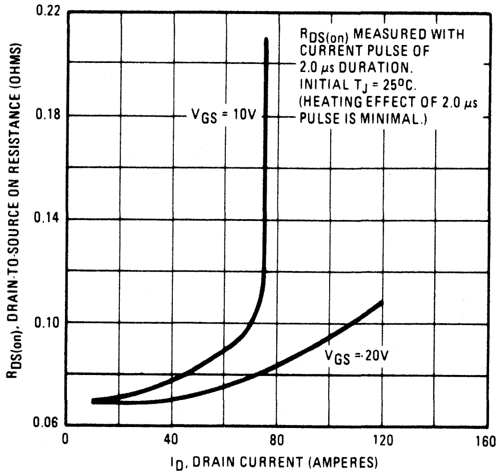


Fig. 12 – Typical On-Resistance Vs. Drain Current

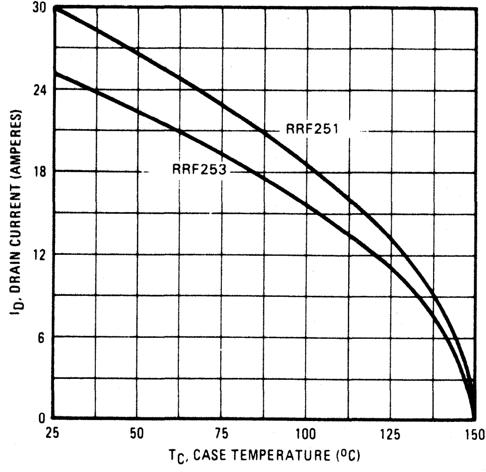


Fig. 13 – Maximum Drain Current Vs. Case Temperature

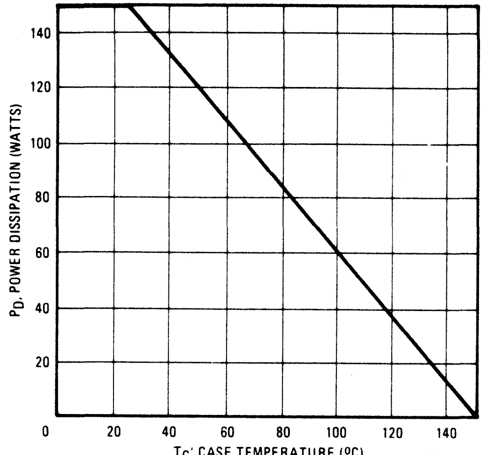


Fig. 14 – Power Vs. Temperature Derating Curve

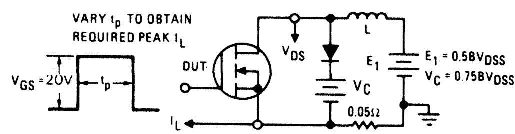


Fig. 15 – Clamped Inductive Test Circuit

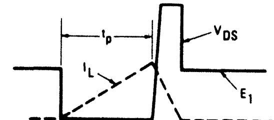


Fig. 16 – Clamped Inductive Waveforms

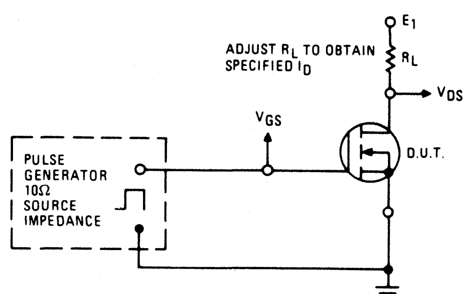


Fig. 17 – Switching Time Test Circuit

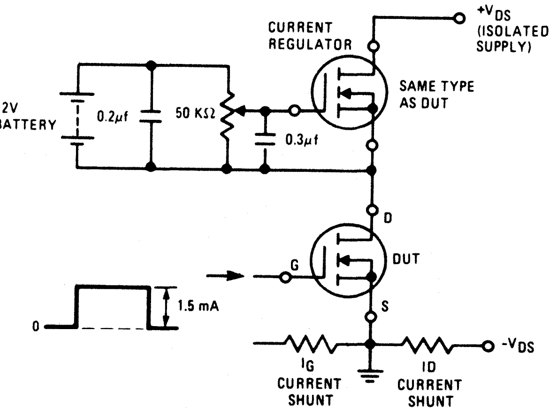


Fig. 18 – Gate Charge Test Circuit

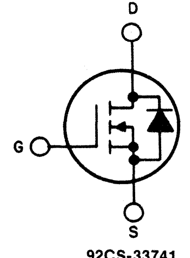
RRF320, RRF321, RRF322, RRF323 *

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

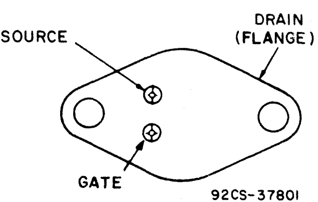
$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-204AA

The RRF320, RRF321, RRF322 and RRF323* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF320, IRF321, IRF322 and IRF323, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF320	RRF321	RRF322	RRF323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 12	12	10	10	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

RRF320, RRF321, RRF322, RRF323

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF320 RRF322	400	–	–	V	V_{GS} = 0V
		RRF321 RRF323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF320 RRF321	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF322 RRF323	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF320 RRF321	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		RRF322 RRF323	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

D, LD, G, LS, S

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF320 RRF321	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF322 RRF323	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF320 RRF321	–	–	12	A	
		RRF322 RRF323	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	RRF320 RRF321	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		RRF322 RRF323	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2% ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

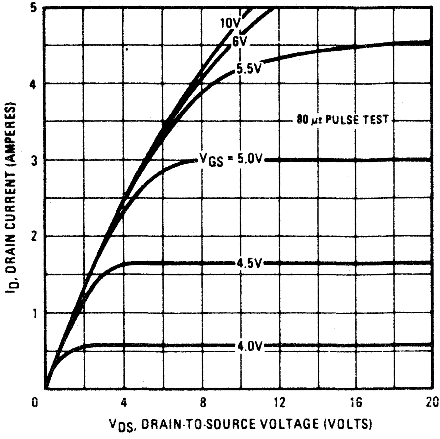


Fig. 1 — Typical Output Characteristics

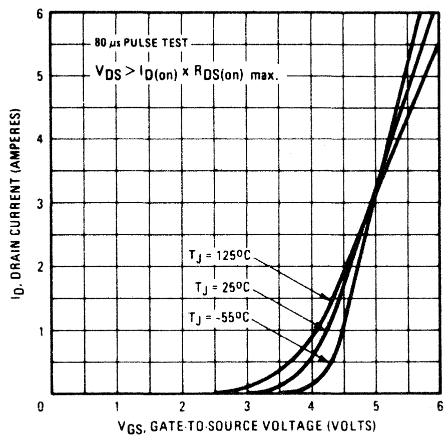


Fig. 2 — Typical Transfer Characteristics

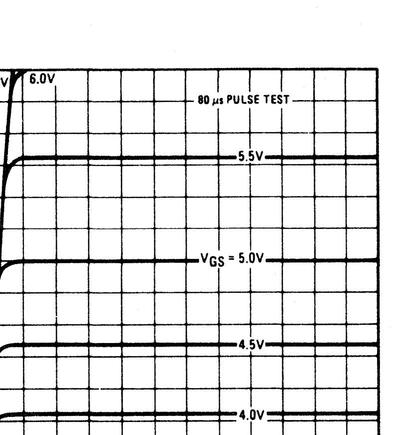


Fig. 3 — Typical Saturation Characteristics

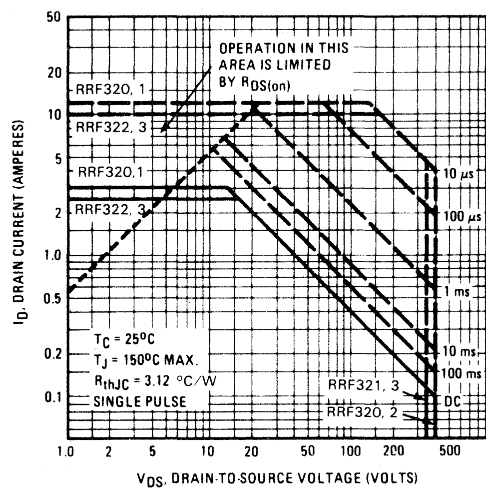


Fig. 4 — Maximum Safe Operating Area

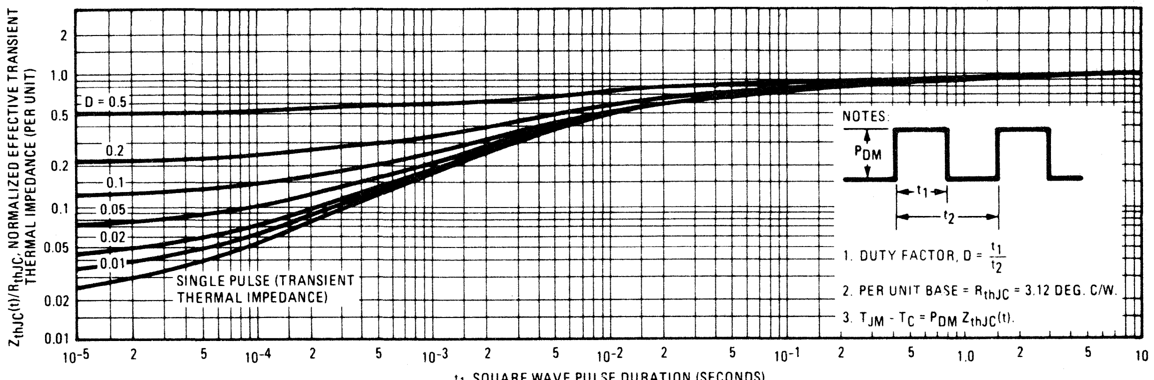


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

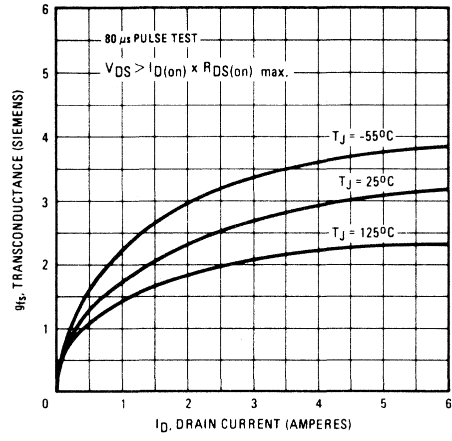


Fig. 6 — Typical Transconductance Vs. Drain Current

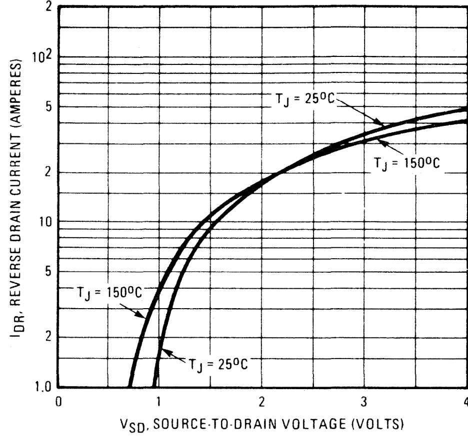


Fig. 7 — Typical Source-Drain Diode Forward Voltage

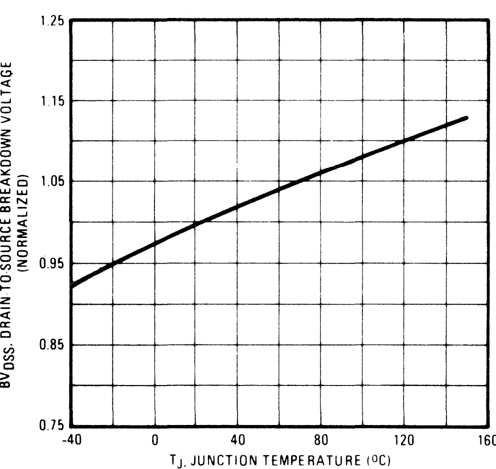


Fig. 8 — Breakdown Voltage Vs. Temperature

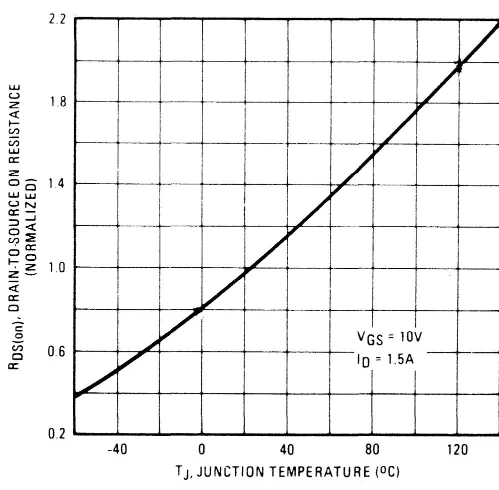


Fig. 9 — Normalized On-Resistance Vs. Temperature

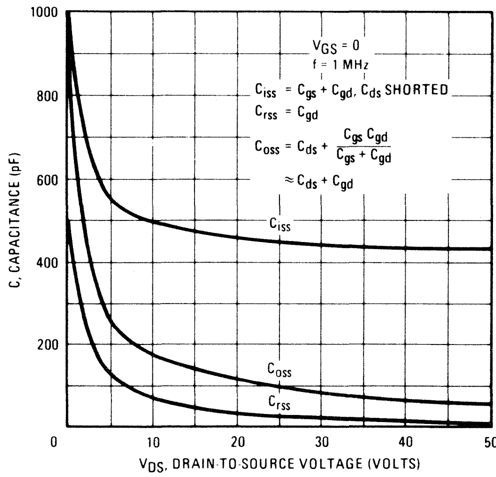


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

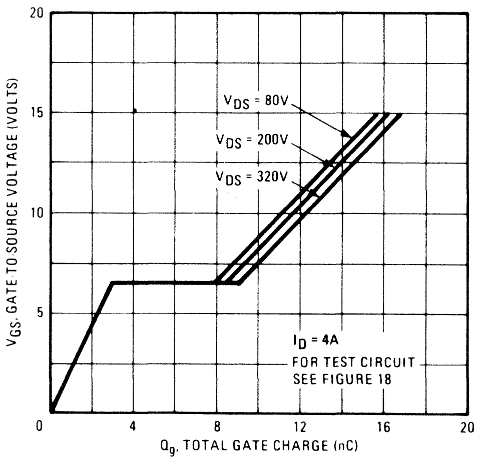


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

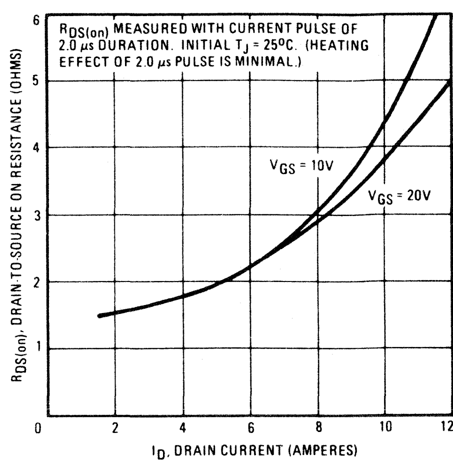


Fig. 12 – Typical On-Resistance Vs. Drain Current

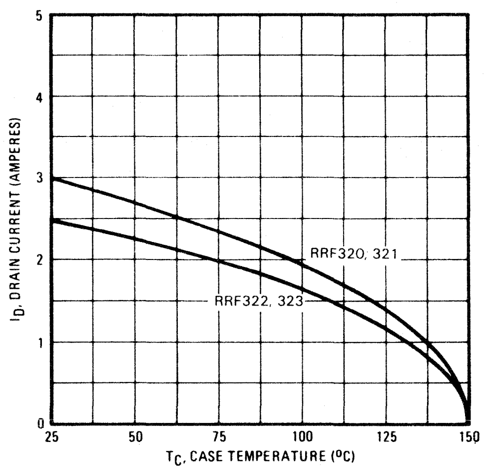


Fig. 13 – Maximum Drain Current Vs. Case Temperature

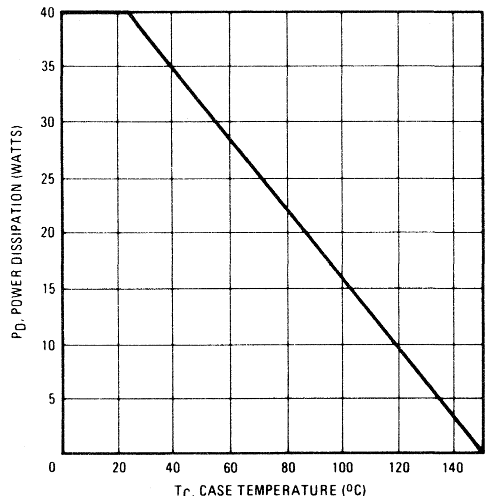


Fig. 14 – Power Vs. Temperature Derating Curve

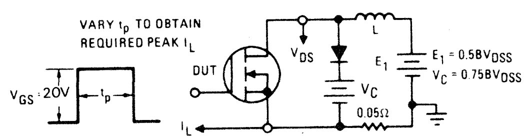


Fig. 15 – Clamped Inductive Test Circuit

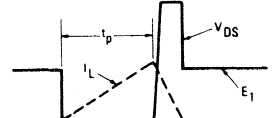


Fig. 16 – Clamped Inductive Waveforms

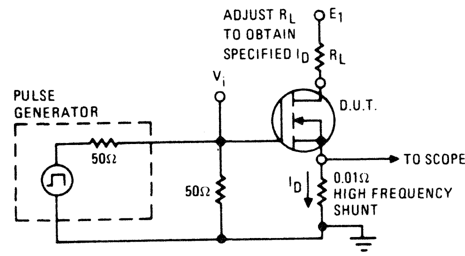


Fig. 17 – Switching Time Test Circuit

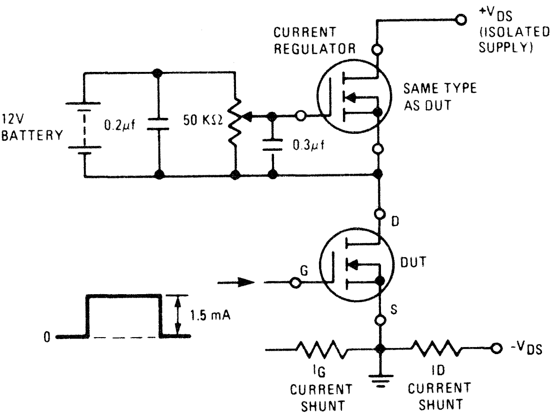


Fig. 18 – Gate Charge Test Circuit

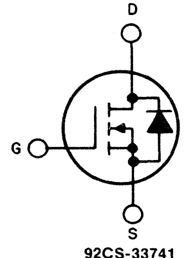
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



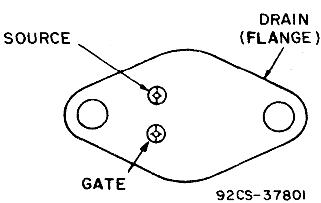
N-CHANNEL ENHANCEMENT MODE

The RRF330, RRF331, RRF332 and RRF333* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF330, IRF331, IRF332 and IRF333, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

	Parameter	RRF330	RRF331	RRF332	RRF333	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22	22	18	18	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF330 RRF332	400	–	–	V	V_{GS} = 0V
		RRF331 RRF333	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF330 RRF331	5.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF332 RRF333	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF330 RRF331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		RRF332 RRF333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF330 RRF331	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF332 RRF333	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF330 RRF331	–	–	22	A	
		RRF332 RRF333	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	RRF330 RRF331	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		RRF332 RRF333	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

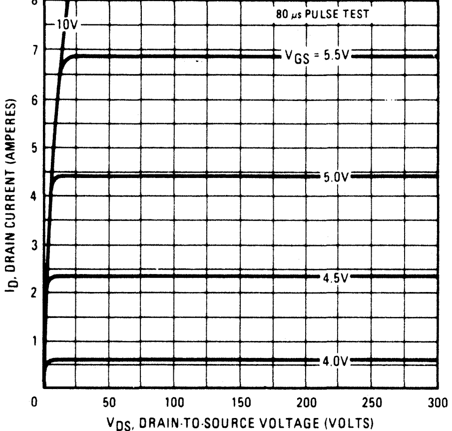


Fig. 1 — Typical Output Characteristics

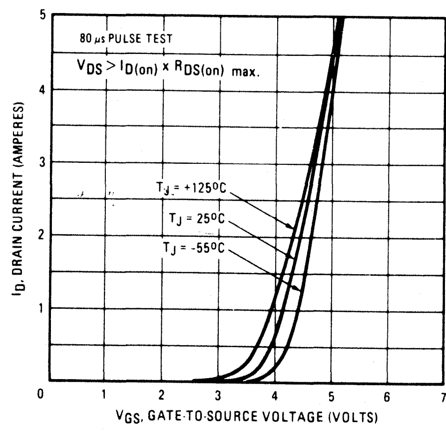


Fig. 2 — Typical Transfer Characteristics

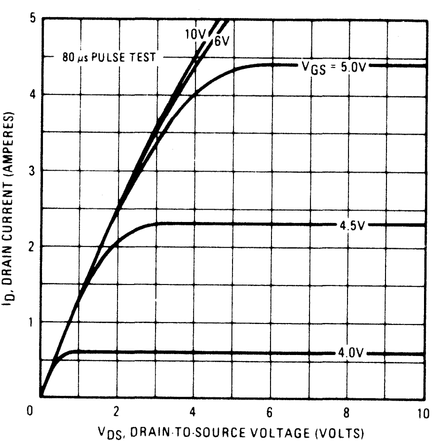


Fig. 3 — Typical Saturation Characteristics

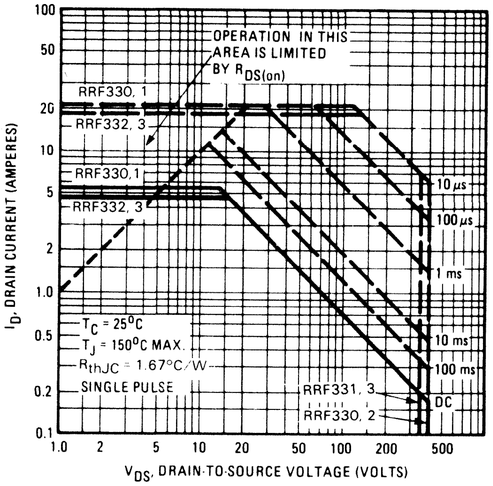


Fig. 4 — Maximum Safe Operating Area

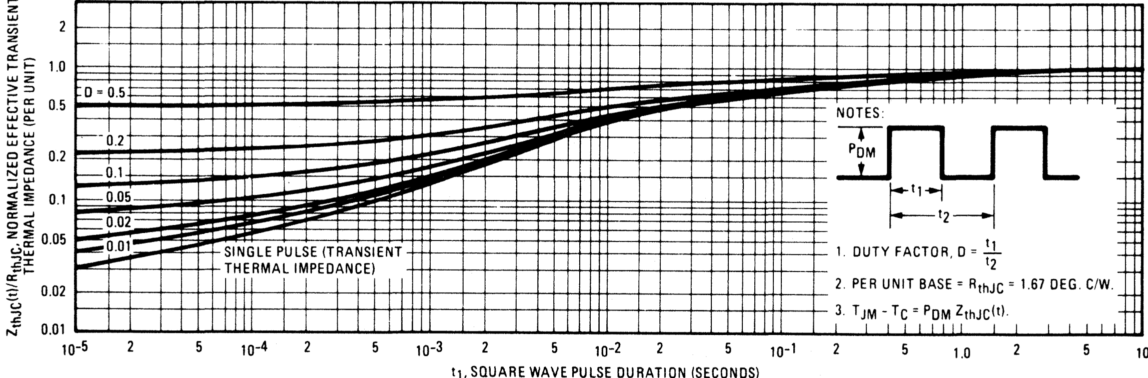


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

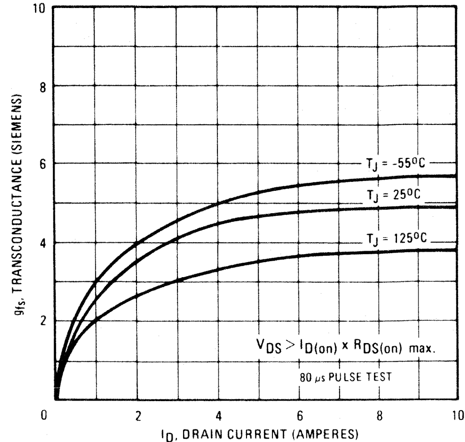


Fig. 6 — Typical Transconductance Vs. Drain Current

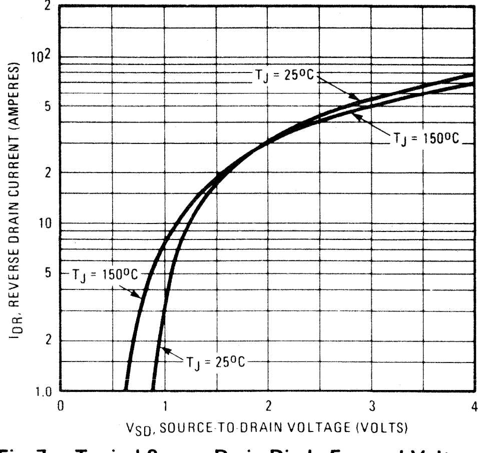


Fig. 7 — Typical Source-Drain Diode Forward Voltage

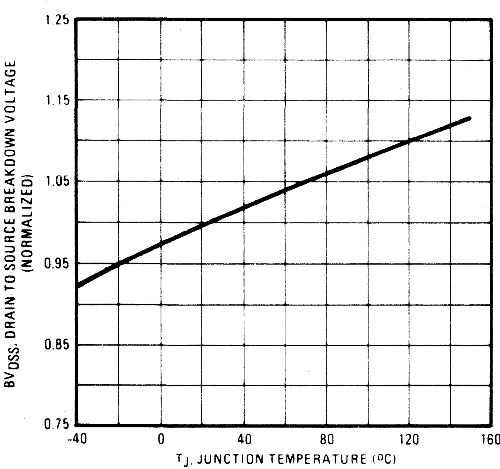


Fig. 8 — Breakdown Voltage Vs. Temperature

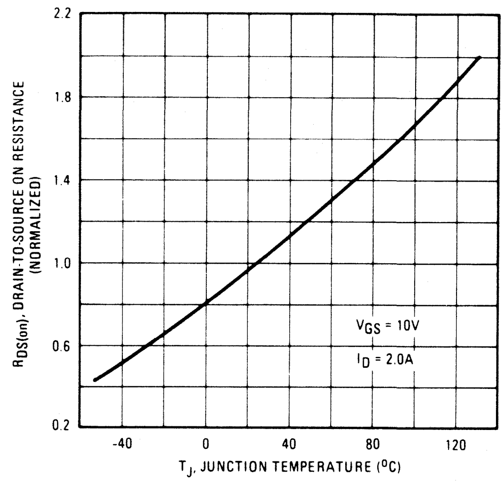


Fig. 9 — Normalized On-Resistance Vs. Temperature

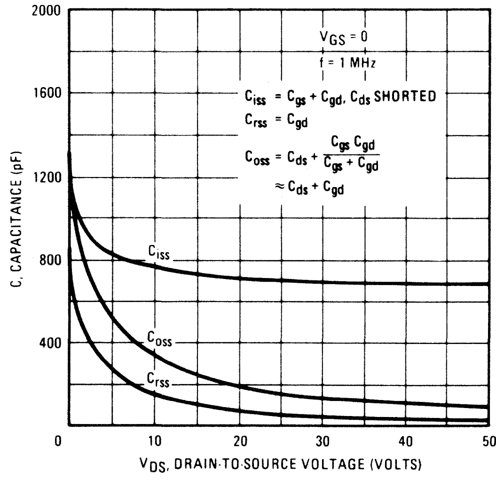


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

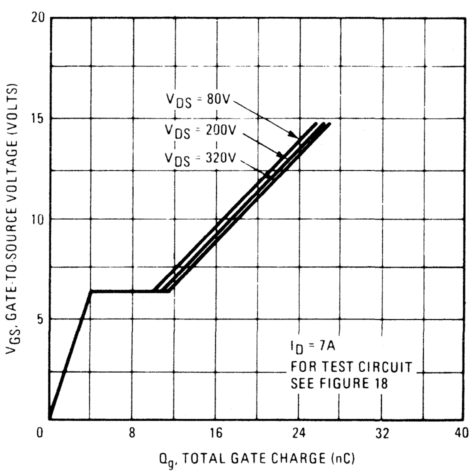


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

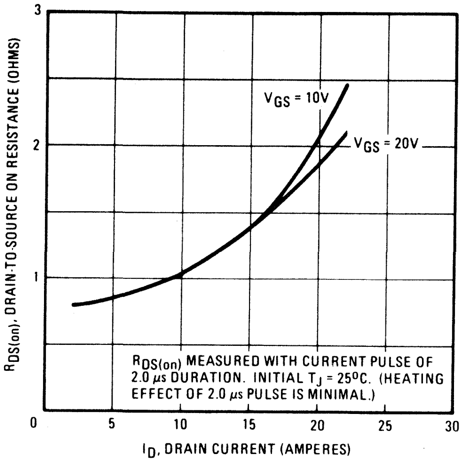


Fig. 12 – Typical On-Resistance Vs. Drain Current

RRF330, 331
RRF332, 333
I_D, DRAIN CURRENT (AMPERES)
T_C, CASE TEMPERATURE (°C)
0 2 4 6 8 10
25 50 75 100 125 150

Fig. 13 – Maximum Drain Current Vs. Case Temperature

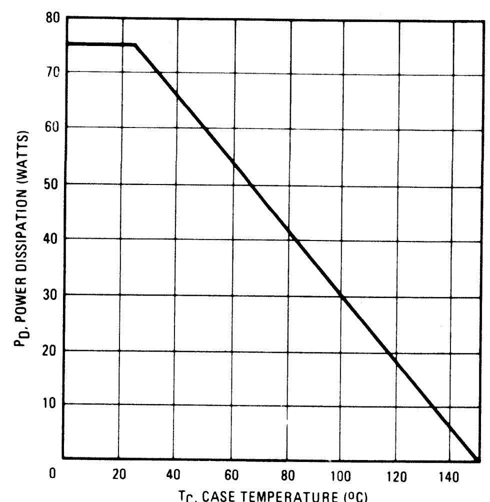


Fig. 14 – Power Vs. Temperature Derating Curve

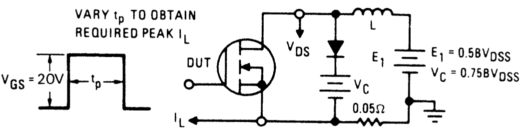


Fig. 15 – Clamped Inductive Test Circuit

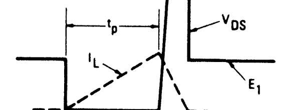


Fig. 16 – Clamped Inductive Waveforms

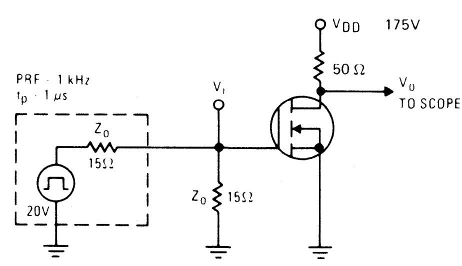


Fig. 17 – Switching Time Test Circuit

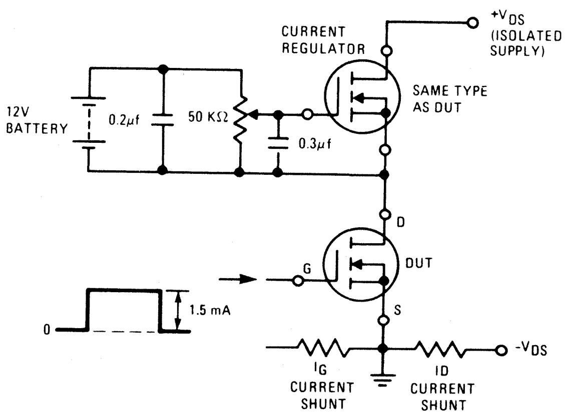


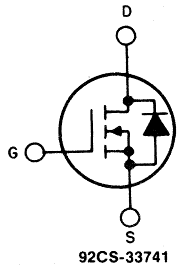
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



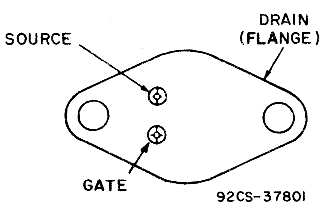
N-CHANNEL ENHANCEMENT MODE

The RRF420, RRF421, RRF422 and RRF423* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF420, IRF421, IRF422 and IRF423, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

	Parameter	RRF420	RRF421	RRF422	RRF423	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

RRF420, RRF421, RRF422, RRF423

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF420 RRF422	500	–	–	V	V_{GS} = 0V
		RRF421 RRF423	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF420 RRF421	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		RRF422 RRF423	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF420 RRF421	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		RRF422 RRF423	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF420 RRF421	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF422 RRF423	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF420 RRF421	–	–	10	A	
		RRF422 RRF423	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	RRF420 RRF421	–	–	1.4	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		RRF422 RRF423	–	–	1.3	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

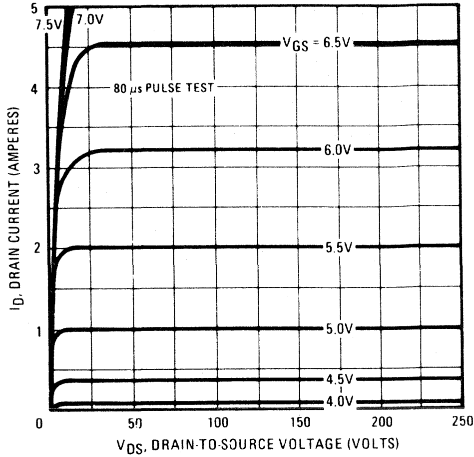


Fig. 1 — Typical Output Characteristics

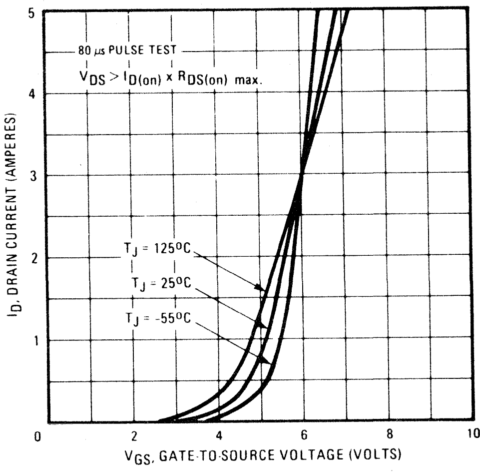


Fig. 2 — Typical Transfer Characteristics

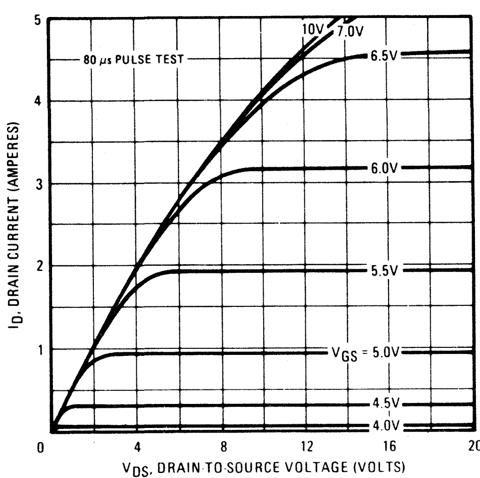


Fig. 3 — Typical Saturation Characteristics

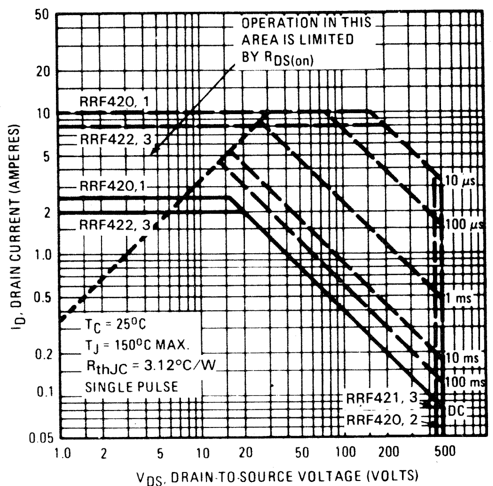


Fig. 4 — Maximum Safe Operating Area

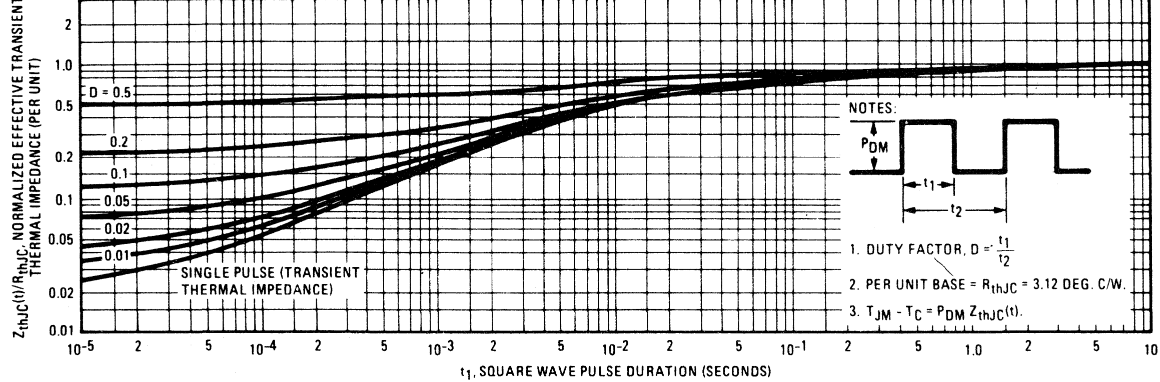


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

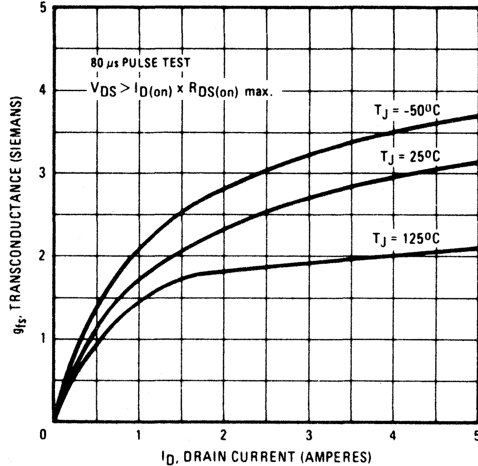


Fig. 6 — Typical Transconductance Vs. Drain Current

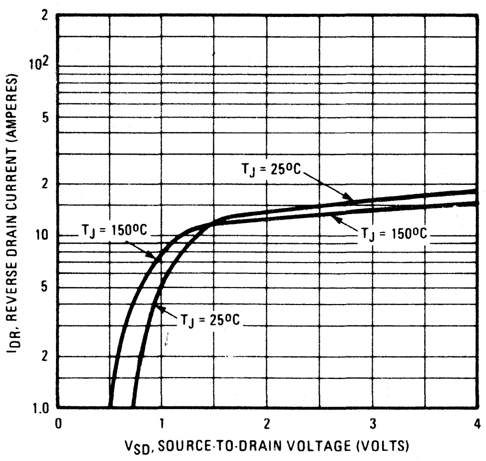


Fig. 7 — Typical Source-Drain Diode Forward Voltage

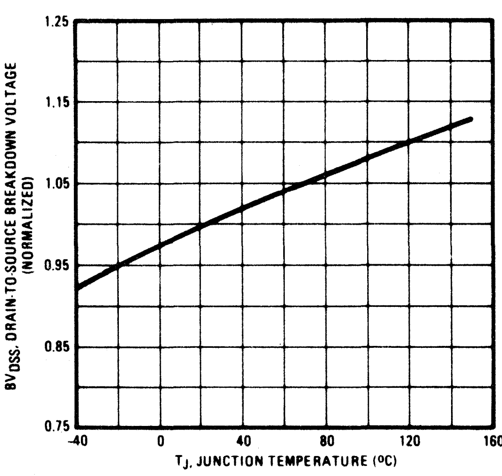


Fig. 8 — Breakdown Voltage Vs. Temperature

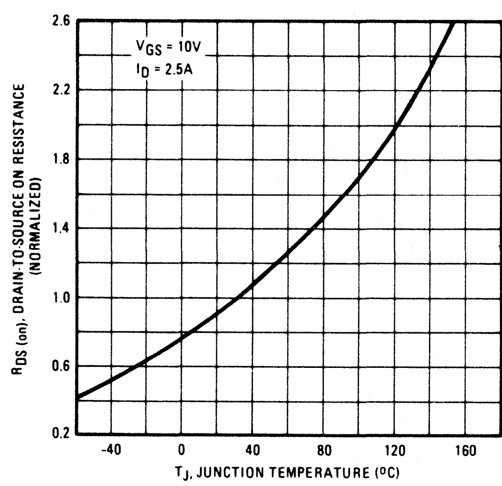


Fig. 9 — Normalized On-Resistance Vs. Temperature

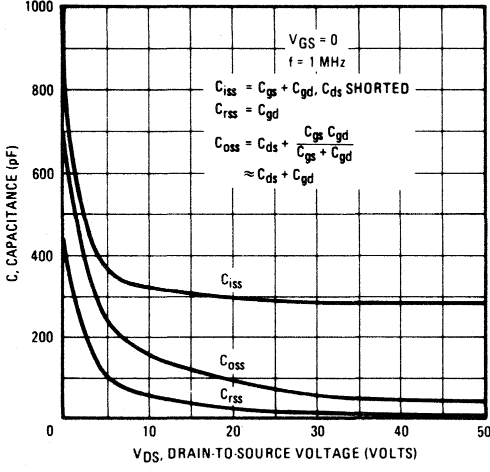


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

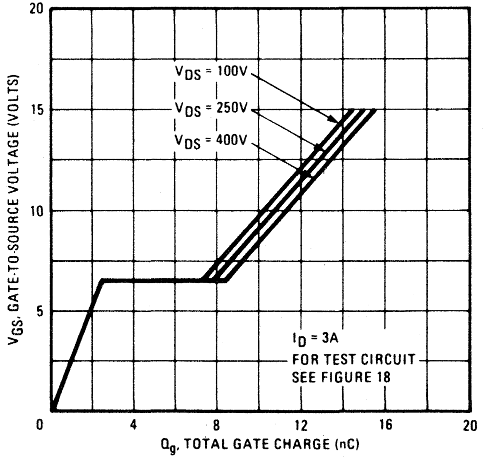


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

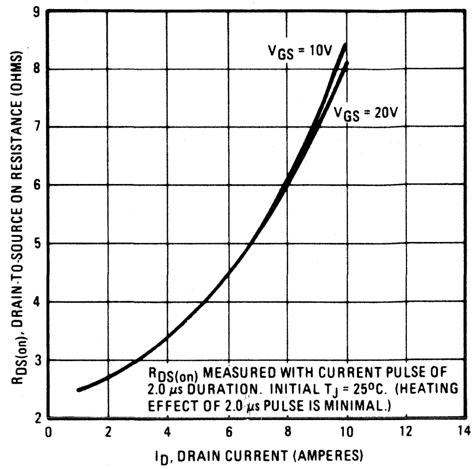


Fig. 12 – Typical On-Resistance Vs. Drain Current

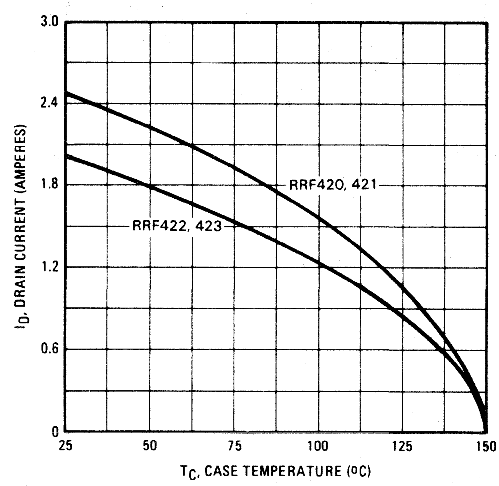


Fig. 13 – Maximum Drain Current Vs. Case Temperature

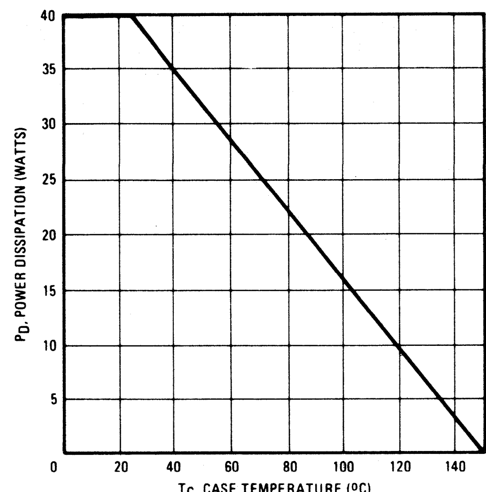


Fig. 14 – Power Vs. Temperature Derating Curve

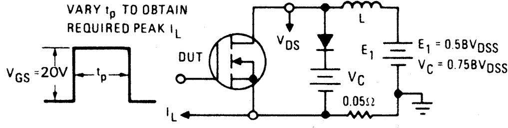


Fig. 15 – Clamped Inductive Test Circuit

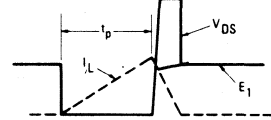


Fig. 16 – Clamped Inductive Waveforms

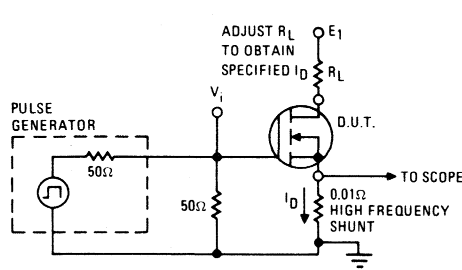


Fig. 17 – Switching Time Test Circuit

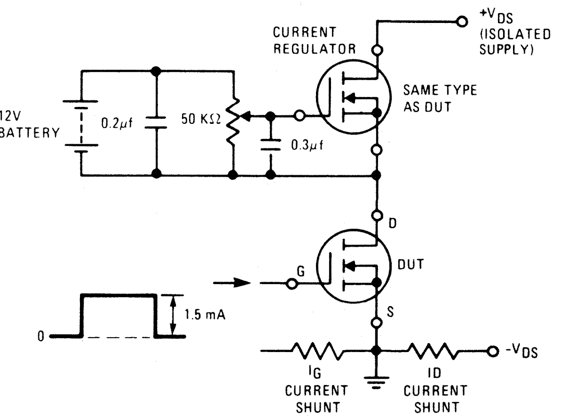


Fig. 18 – Gate Charge Test Circuit

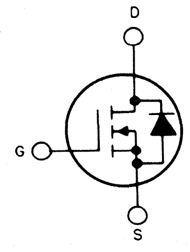
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



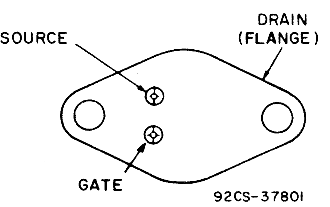
N-CHANNEL ENHANCEMENT MODE

The RRF430, RRF431, RRF432 and RRF433* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-204AA steel package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF430, IRF431, IRF432 and IRF433, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

	Parameter	RRF430	RRF431	RRF432	RRF433	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 18	18	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF430 RRF432	500	–	–	V	V_{GS} = 0V
		RRF431 RRF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF430 RRF431	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		RRF432 RRF433	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF430 RRF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		RRF432 RRF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 225V, I_D = 2.5A, Z_O = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF430 RRF431	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF432 RRF433	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF430 RRF431	–	–	18	A	
		RRF432 RRF433	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	RRF430 RRF431	–	–	1.4	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		RRF432 RRF433	–	–	1.3	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

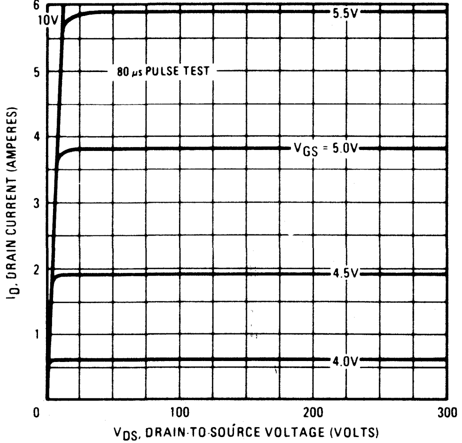


Fig. 1 — Typical Output Characteristics

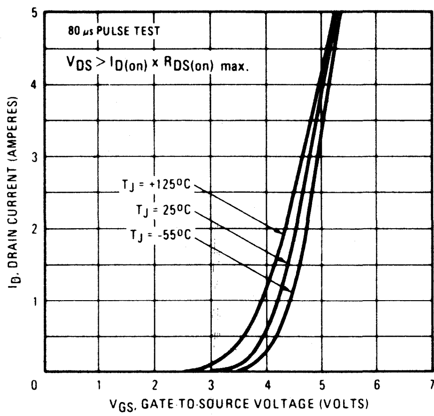


Fig. 2 — Typical Transfer Characteristics

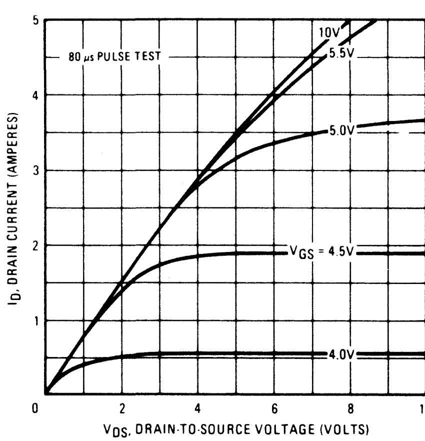


Fig. 3 — Typical Saturation Characteristics

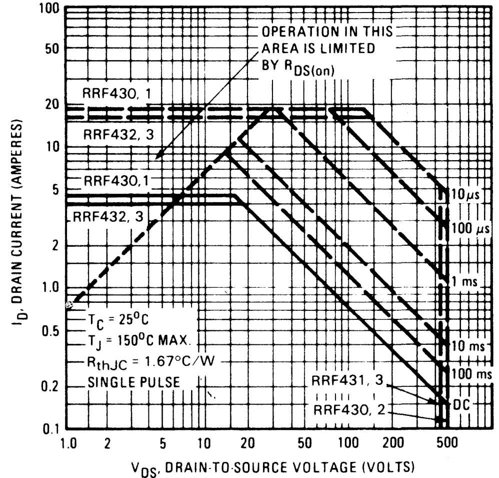


Fig. 4 — Maximum Safe Operating Area

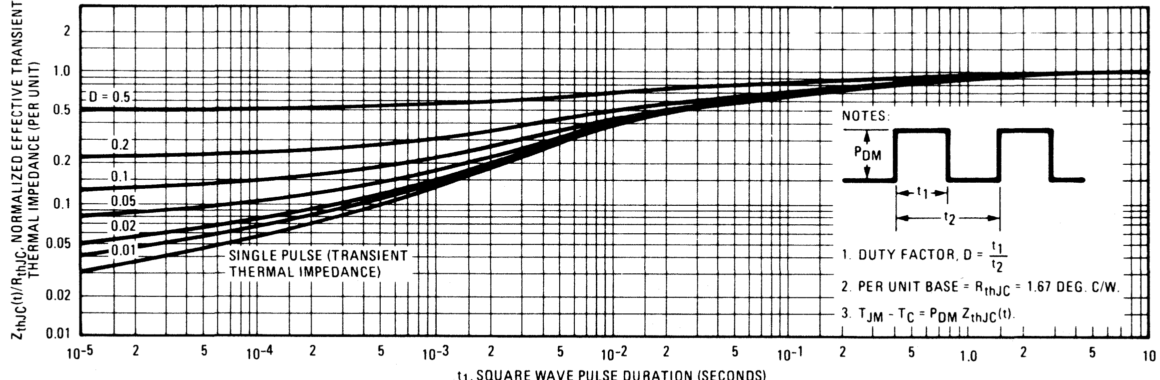


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

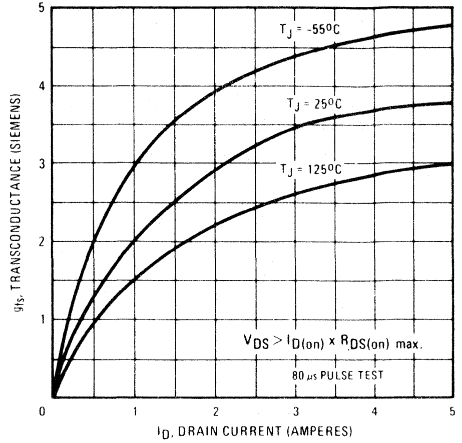


Fig. 6 — Typical Transconductance Vs. Drain Current

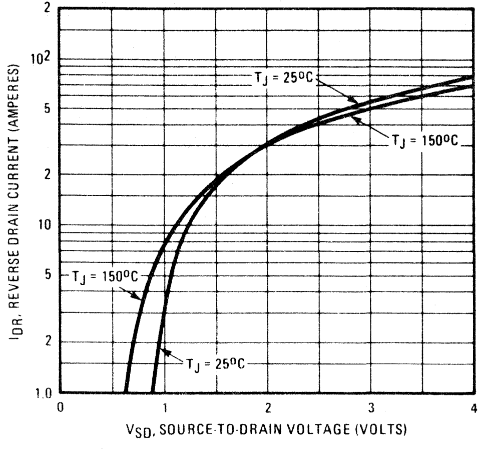


Fig. 7 — Typical Source-Drain Diode Forward Voltage

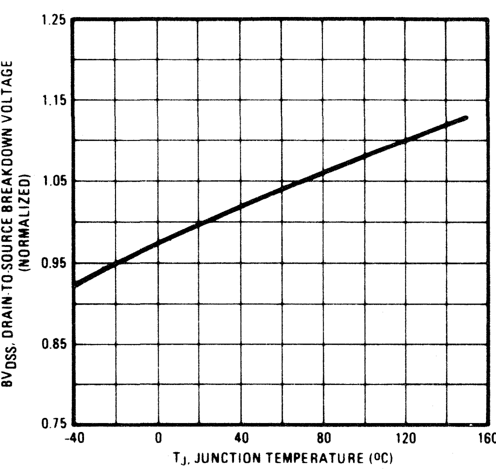


Fig. 8 — Breakdown Voltage Vs. Temperature

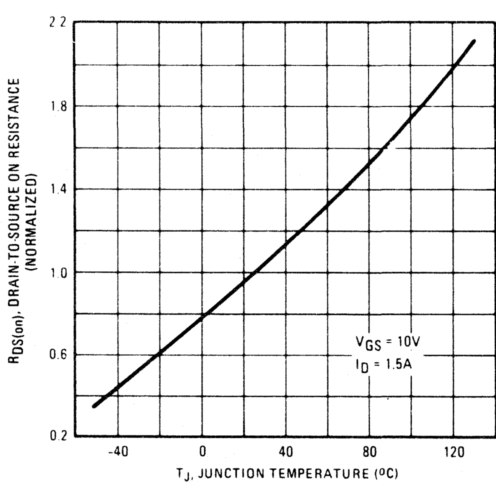


Fig. 9 — Normalized On-Resistance Vs. Temperature

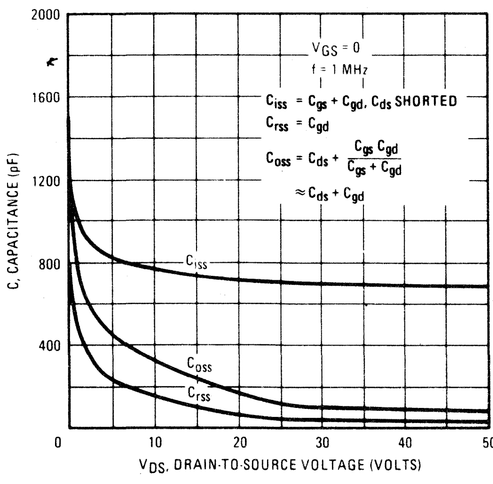


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

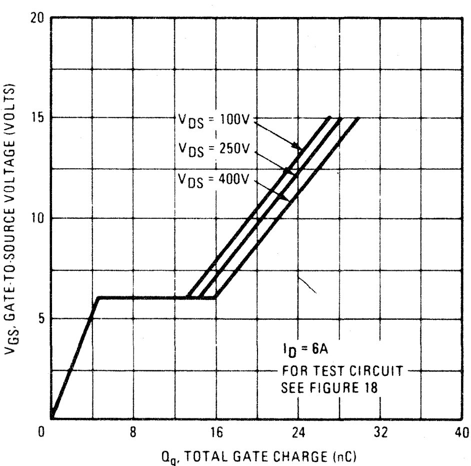


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

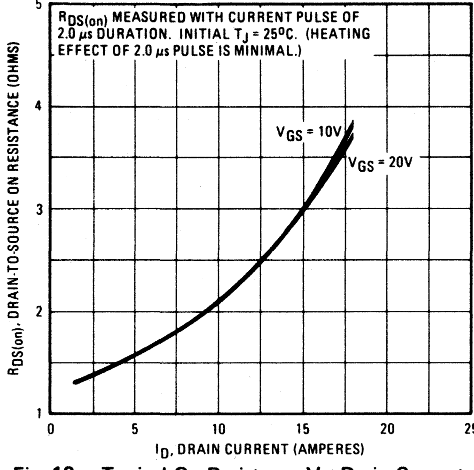


Fig. 12 — Typical On-Resistance Vs. Drain Current

Fig. 13 — Maximum Drain Current Vs. Case Temperature

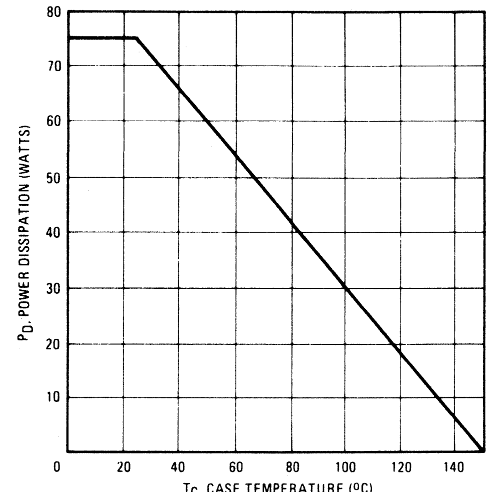


Fig. 14 — Power Vs. Temperature Derating Curve

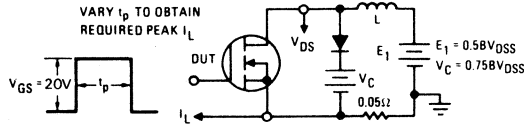


Fig. 15 — Clamped Inductive Test Circuit

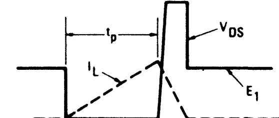


Fig. 16 — Clamped Inductive Waveforms

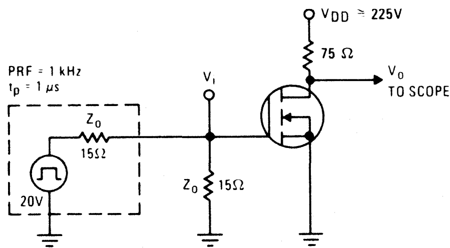


Fig. 17 — Switching Time Test Circuit

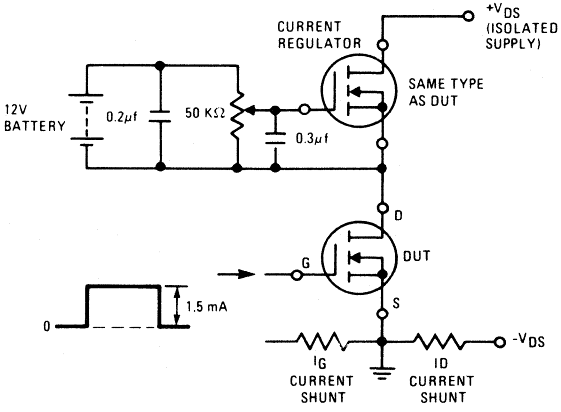


Fig. 18 — Gate Charge Test Circuit

File Number **1573**

RRF510, RRF511, RRF512, RRF513

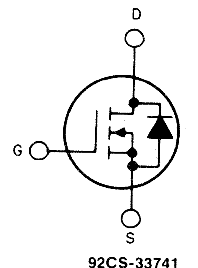
N-Channel Enhancement-Mode Power Field-Effect Transistors

3.5A and 4.0A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



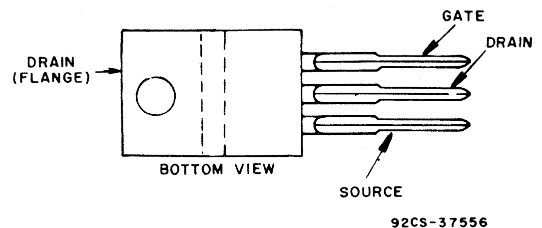
N-CHANNEL ENHANCEMENT MODE

The RRF510, RRF511, RRF512 and RRF513* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF510, IRF511, IRF512 and IRF513, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

Absolute Maximum Ratings

	Parameter	RRF510	RRF511	RRF512	RRF513	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		16	16	14	14	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

RRF510, RRF511, RRF512, RRF513

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF510 RRF512	100	–	–	V	V_{GS} = 0V
		RRF511 RRF513	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF510 RRF511	4.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		RRF512 RRF513	3.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF510 RRF511	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		RRF512 RRF513	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF510 RRF511	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF512 RRF513	–	–	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF510 RRF511	–	–	16	A	
		RRF512 RRF513	–	–	14	A	
V_{SD}	Diode Forward Voltage ②	RRF510 RRF511	–	–	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		RRF512 RRF513	–	–	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.4	–	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

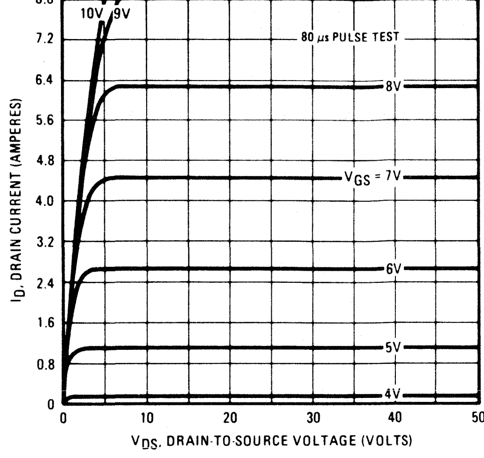


Fig. 1 — Typical Output Characteristics

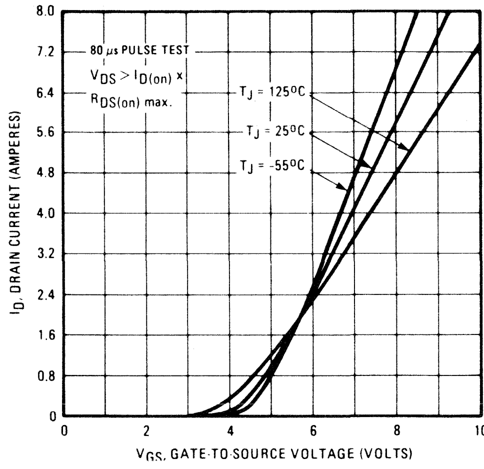


Fig. 2 — Typical Transfer Characteristics

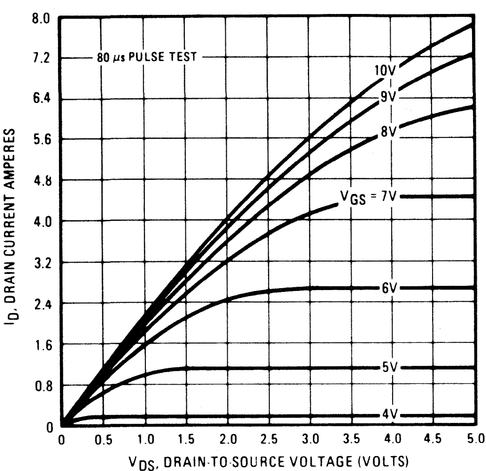


Fig. 3 — Typical Saturation Characteristics

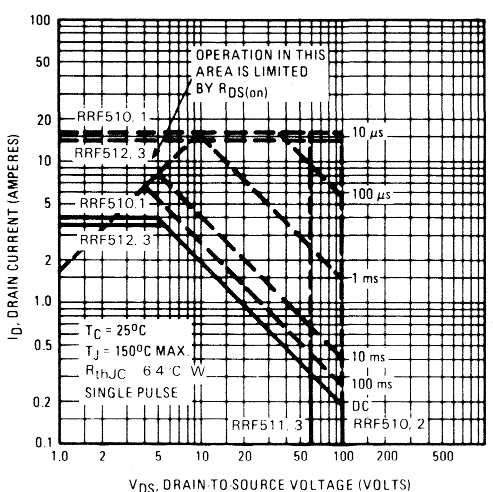


Fig. 4 — Maximum Safe Operating Area

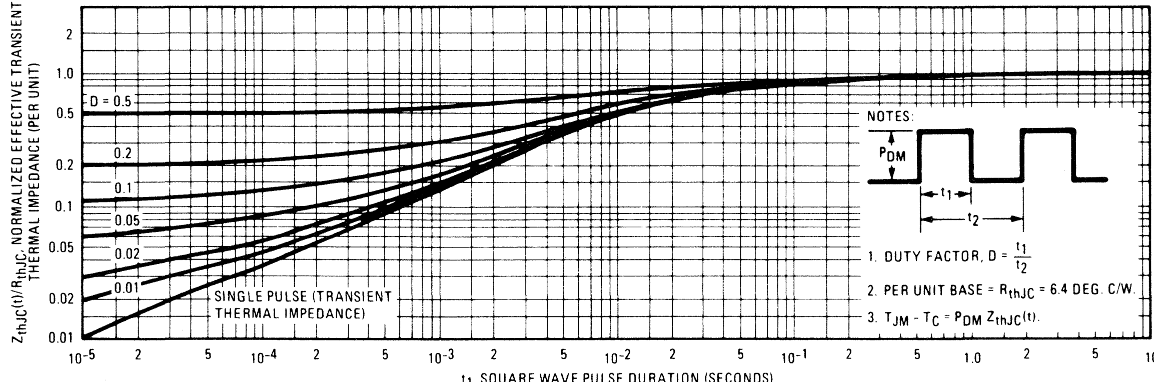


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

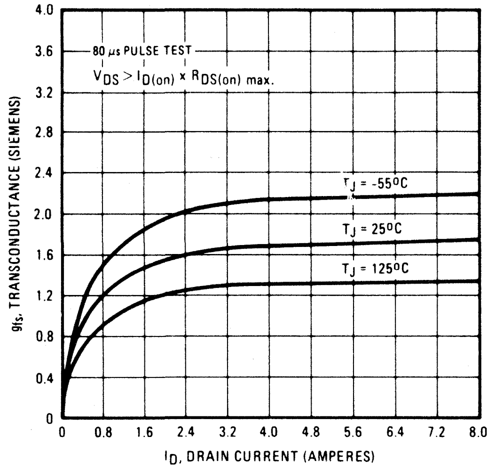


Fig. 6 — Typical Transconductance Vs. Drain Current

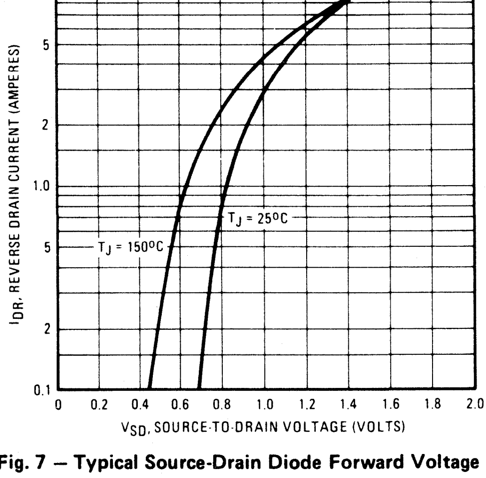


Fig. 7 — Typical Source-Drain Diode Forward Voltage

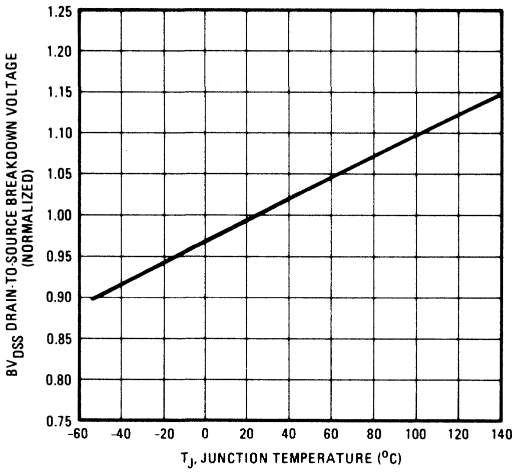


Fig. 8 — Breakdown Voltage Vs. Temperature

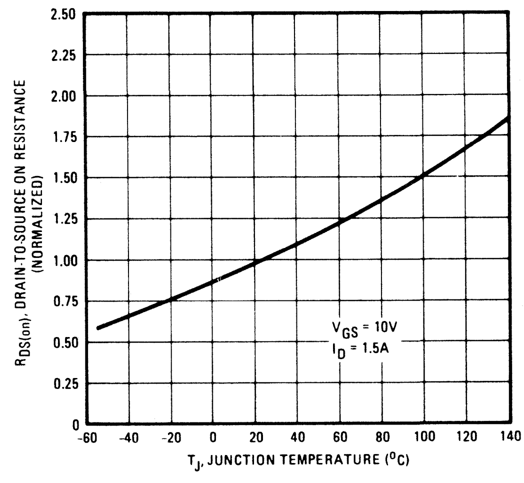


Fig. 9 — Normalized On-Resistance Vs. Temperature

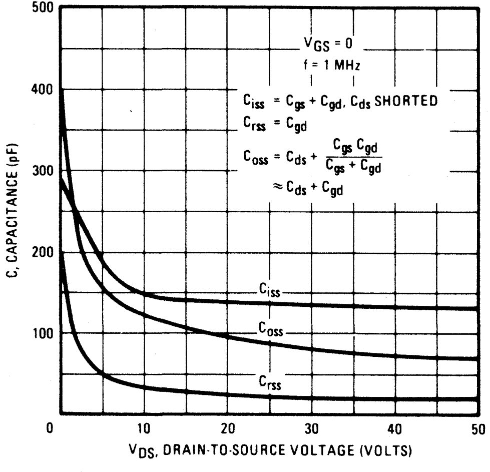


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

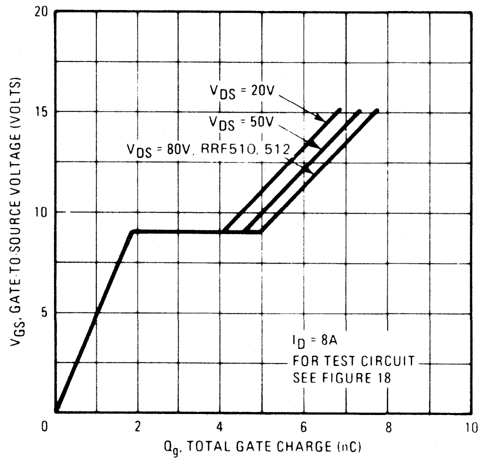


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

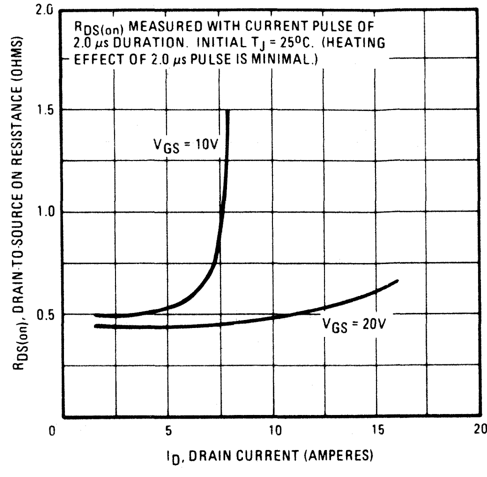


Fig. 12 – Typical On-Resistance Vs. Drain Current

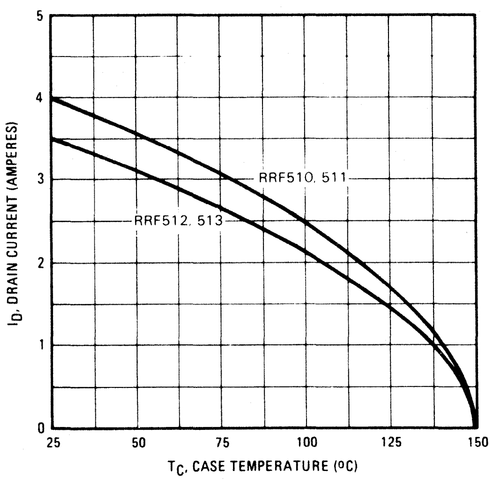


Fig. 13 – Maximum Drain Current Vs. Case Temperature

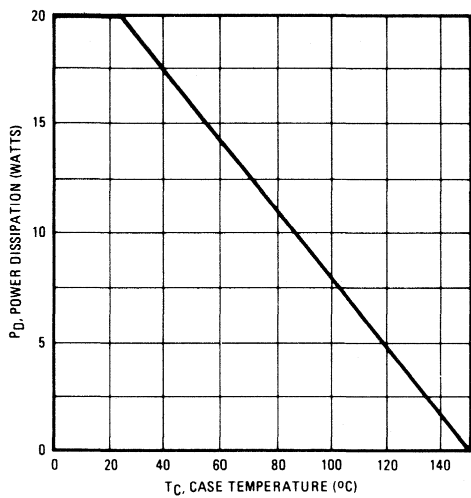


Fig. 14 – Power Vs. Temperature Derating Curve

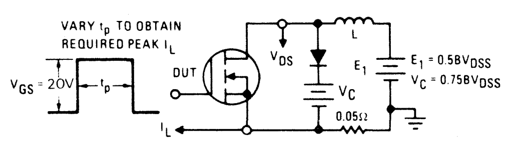


Fig. 15 – Clamped Inductive Test Circuit

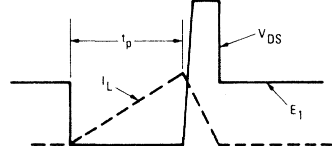


Fig. 16 – Clamped Inductive Waveforms

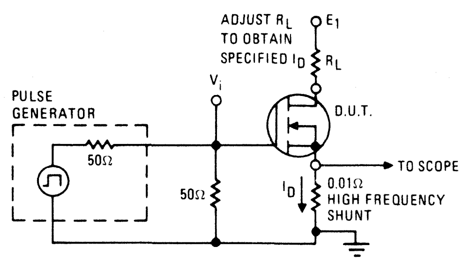


Fig. 17 – Switching Time Test Circuit

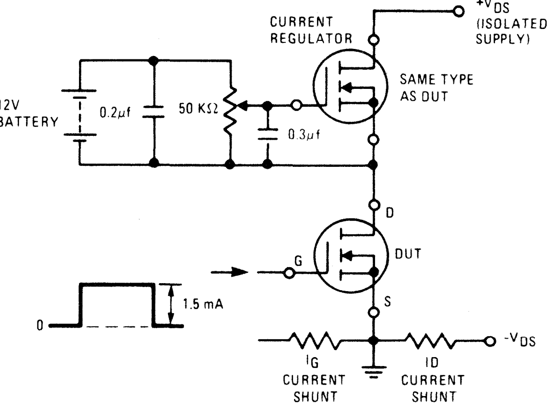


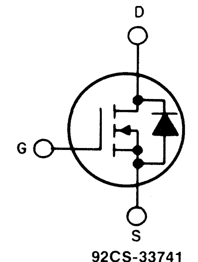
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

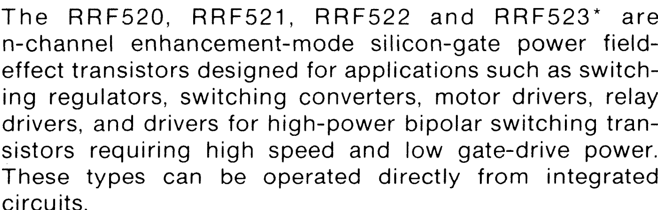
7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

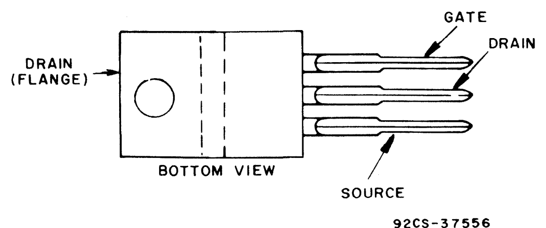


N-CHANNEL ENHANCEMENT MODE


The RRF520, RRF521, RRF522 and RRF523* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

*These devices are equivalent to International Rectifier Power MOSFETs IRF520, IRF521, IRF522 and IRF523, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF520	RRF521	RRF522	RRF523	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF520 RRF522	100	–	–	V	V_{GS} = 0V
		RRF521 RRF523	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF520 RRF521	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF522 RRF523	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF520 RRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		RRF522 RRF523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	3.12	C W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	C W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	C W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF520 RRF521	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF522 RRF523	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF520 RRF521	–	–	32	A	
		RRF522 RRF523	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	RRF520 RRF521	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		RRF522 RRF523	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

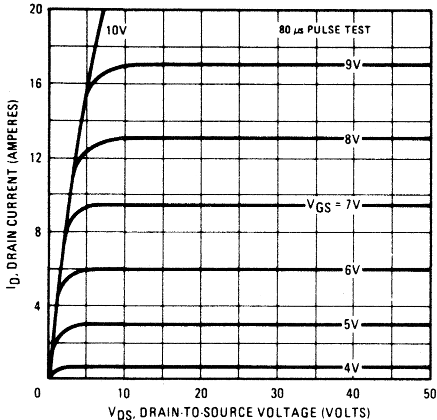


Fig. 1 — Typical Output Characteristics

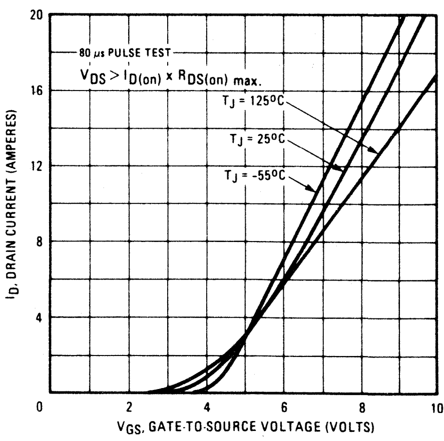


Fig. 2 — Typical Transfer Characteristics

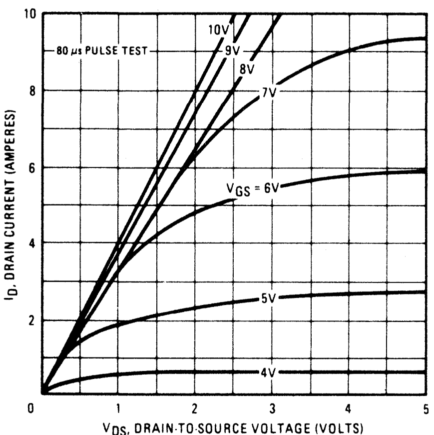


Fig. 3 — Typical Saturation Characteristics

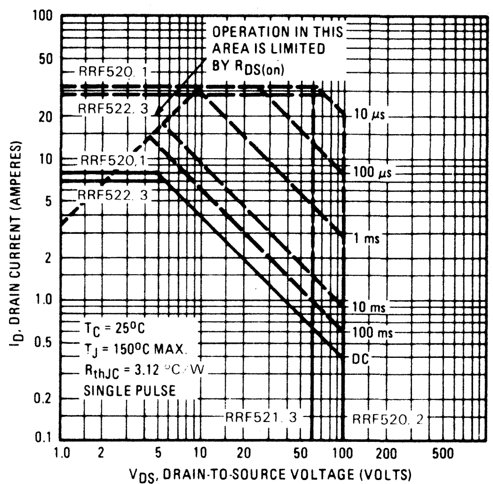


Fig. 4 — Maximum Safe Operating Area

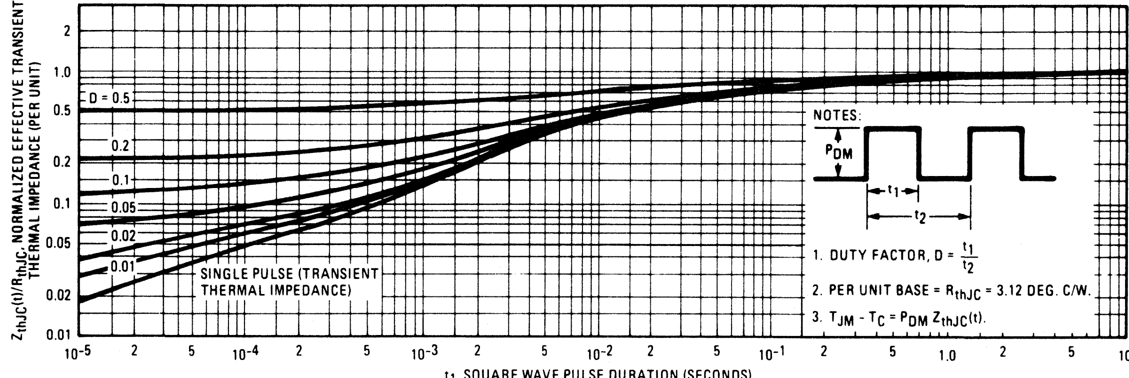


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

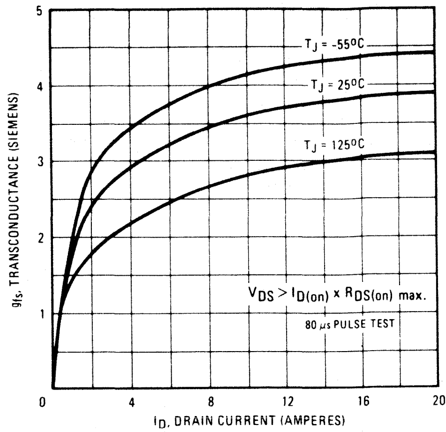


Fig. 6 — Typical Transconductance Vs. Drain Current

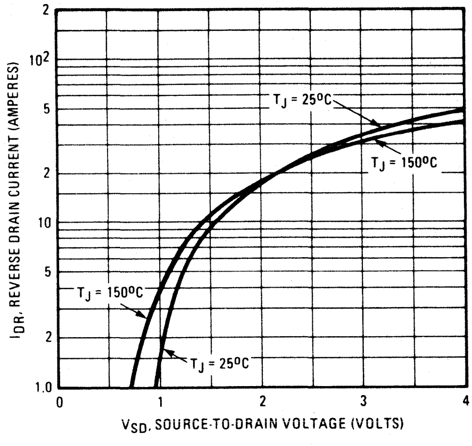


Fig. 7 — Typical Source-Drain Diode Forward Voltage

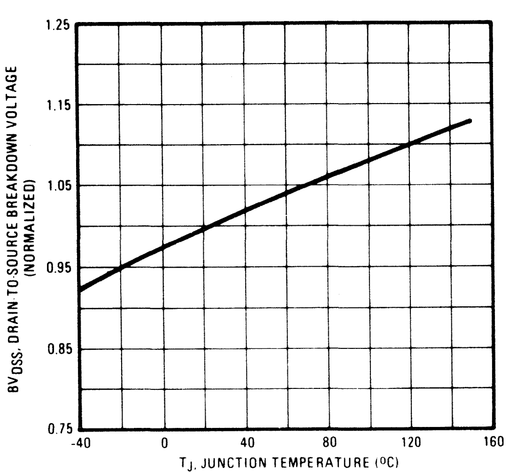


Fig. 8 — Breakdown Voltage Vs. Temperature

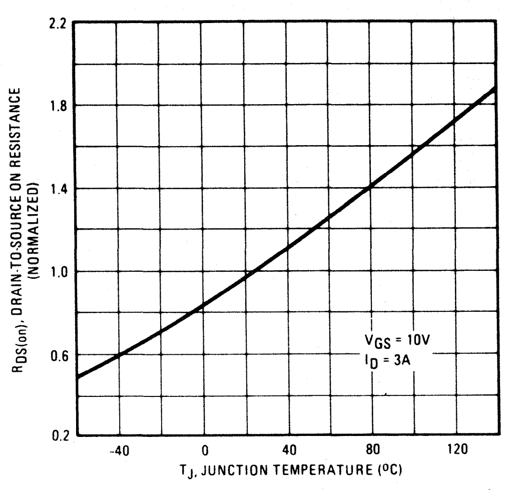


Fig. 9 — Normalized On-Resistance Vs. Temperature

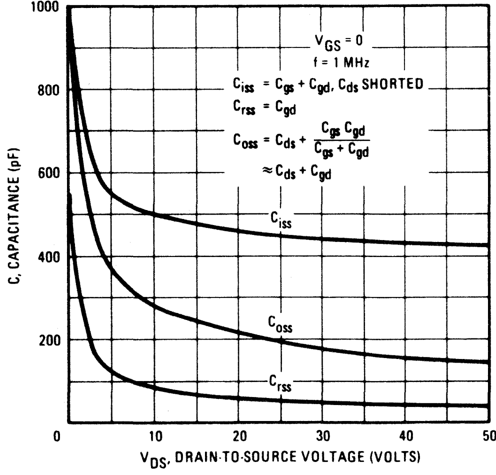


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

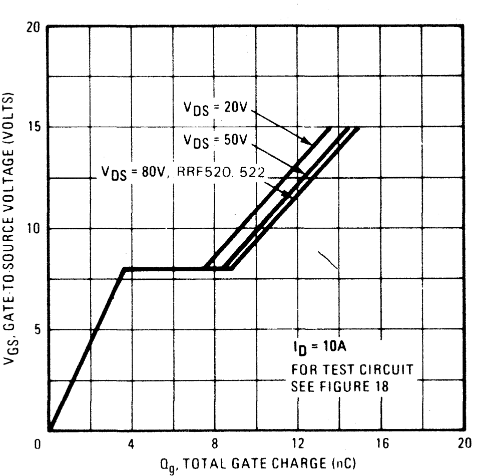


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

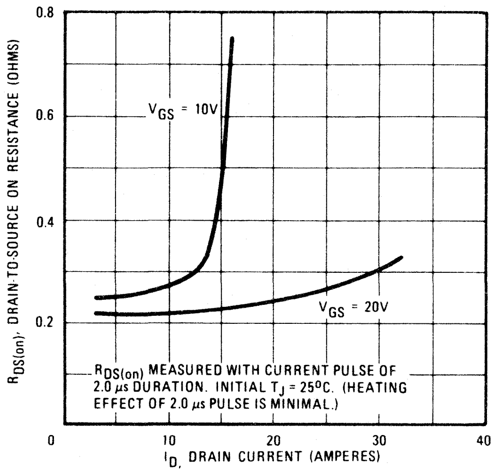


Fig. 12 – Typical On-Resistance Vs. Drain Current

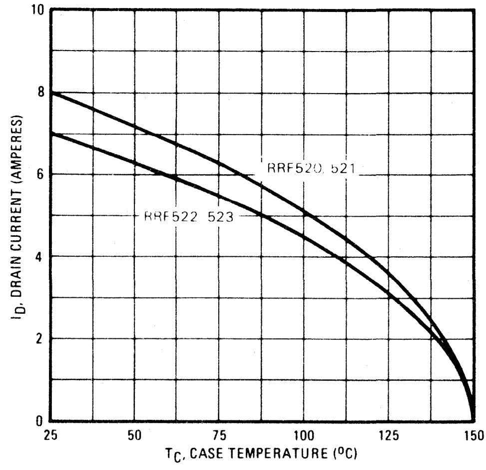


Fig. 13 – Maximum Drain Current Vs. Case Temperature

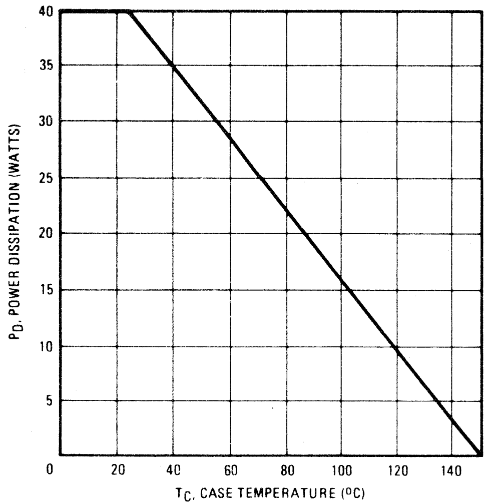


Fig. 14 – Power Vs. Temperature Derating Curve

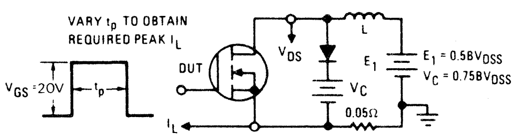


Fig. 15 – Clamped Inductive Test Circuit

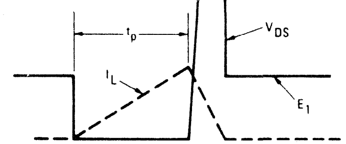


Fig. 16 – Clamped Inductive Waveforms

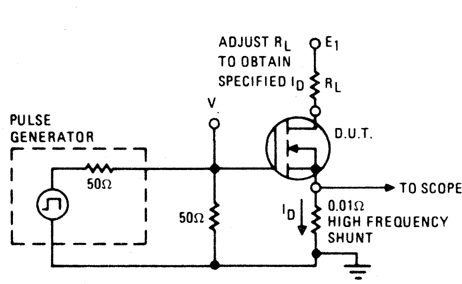


Fig. 17 – Switching Time Test Circuit

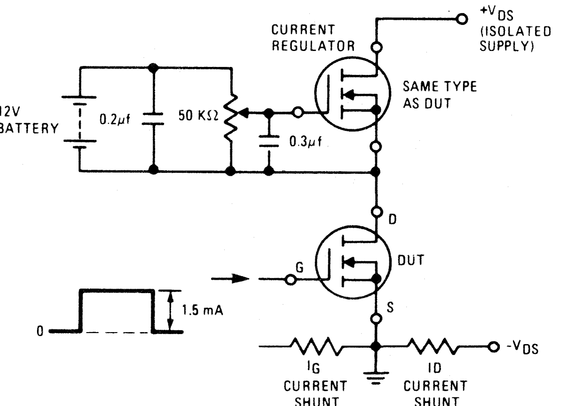


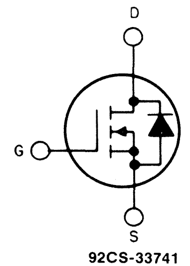
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



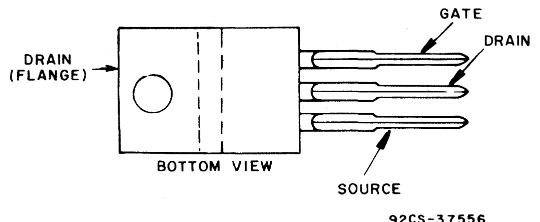
N-CHANNEL ENHANCEMENT MODE

The RRF530, RRF531, RRF532 and RRF533* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF530, IRF531, IRF532 and IRF533, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

Absolute Maximum Ratings

	Parameter	RRF530	RRF531	RRF532	RRF533	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	56	56	48	48	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF530 RRF532	100	–	–	V	V_{GS} = 0V
		RRF531 RRF533	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF530 RRF531	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		RRF532 RRF533	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF530 RRF531	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		RRF532 RRF533	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. / D LD G LS S

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF530 RRF531	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. D G S
		RRF532 RRF533	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF530 RRF531	–	–	56	A	
		RRF532 RRF533	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	RRF530 RRF531	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		RRF532 RRF533	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = -25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

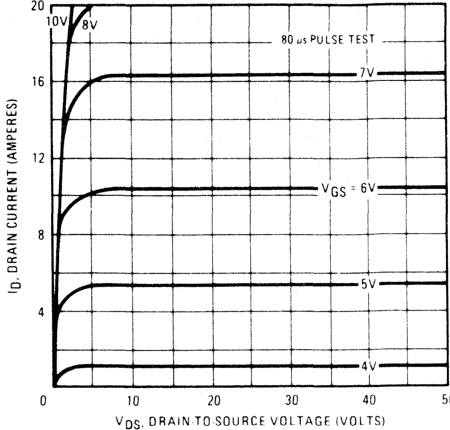


Fig. 1 — Typical Output Characteristics

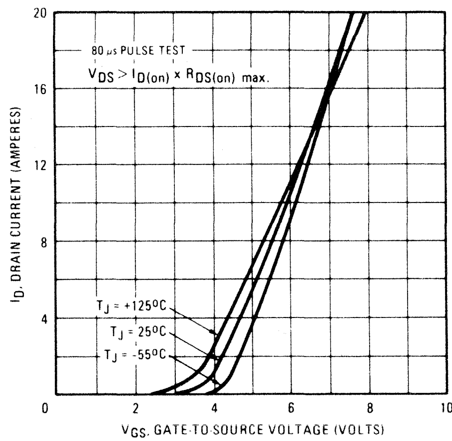


Fig. 2 — Typical Transfer Characteristics

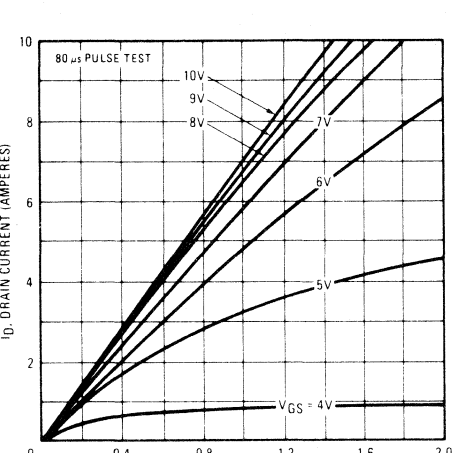


Fig. 3 — Typical Saturation Characteristics

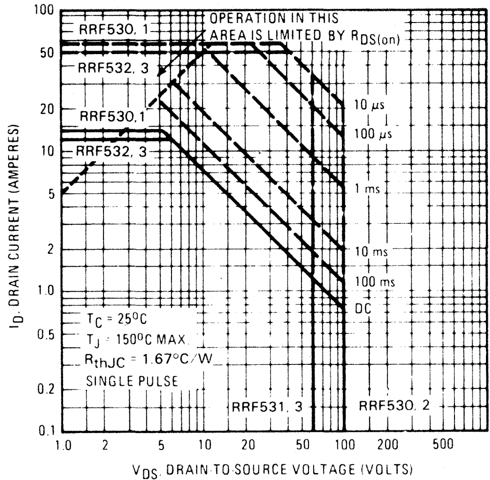


Fig. 4 — Maximum Safe Operating Area

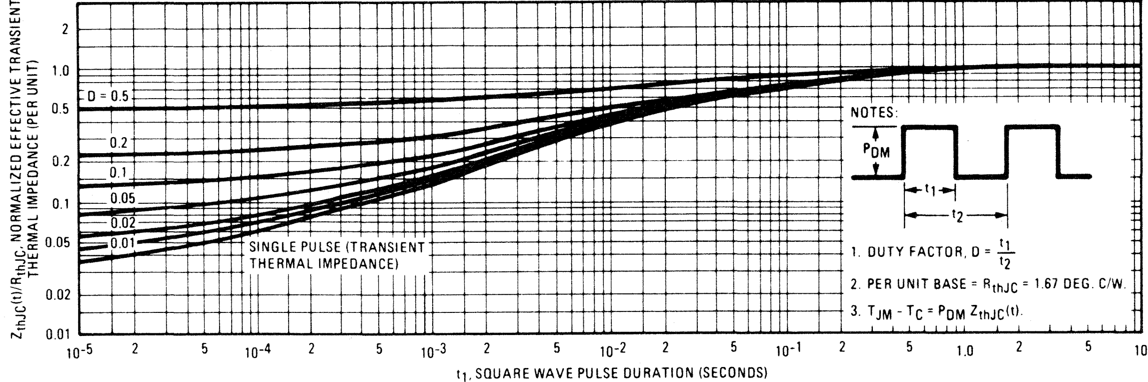


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

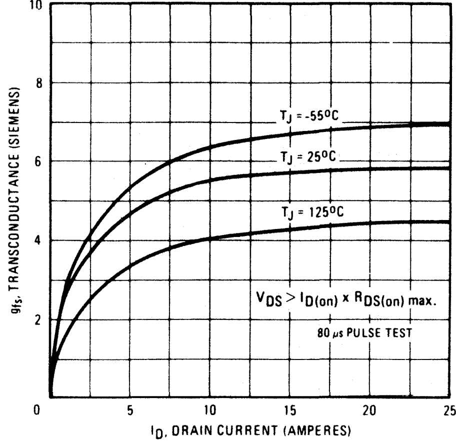


Fig. 6 – Typical Transconductance Vs. Drain Current

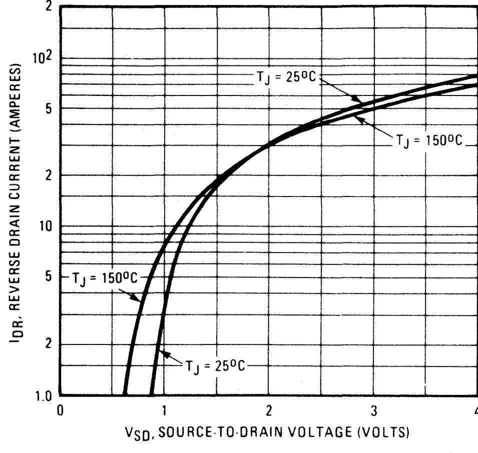


Fig. 7 – Typical Source-Drain Diode Forward Voltage

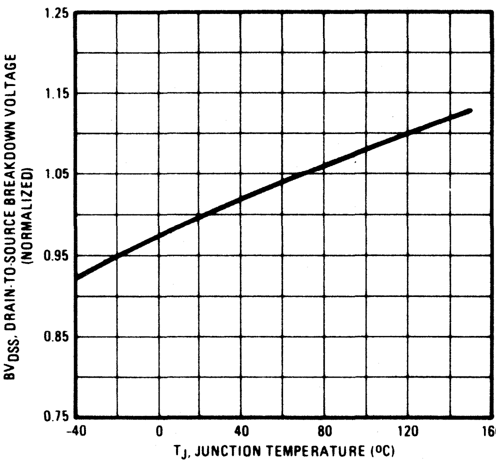


Fig. 8 – Breakdown Voltage Vs. Temperature

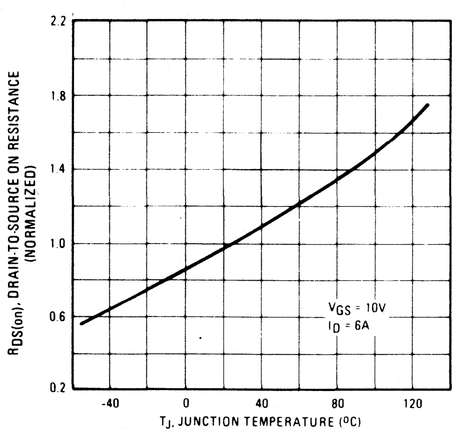


Fig. 9 – Normalized On-Resistance Vs. Temperature

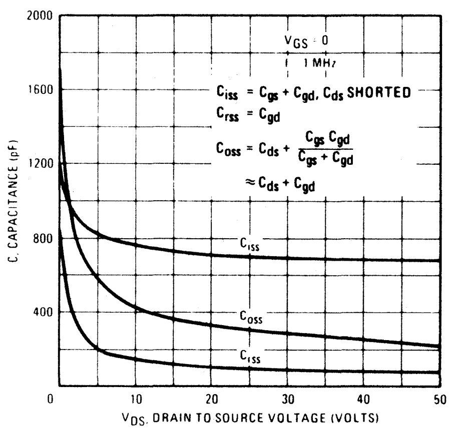


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

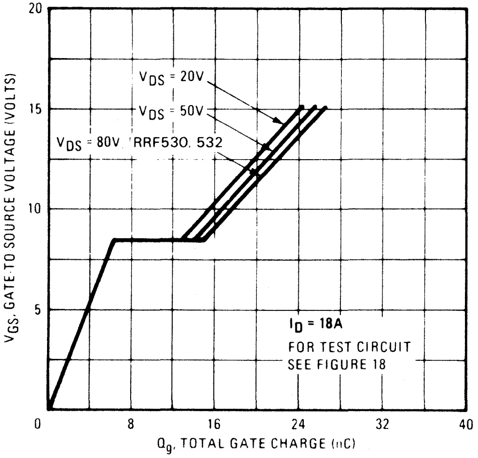


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

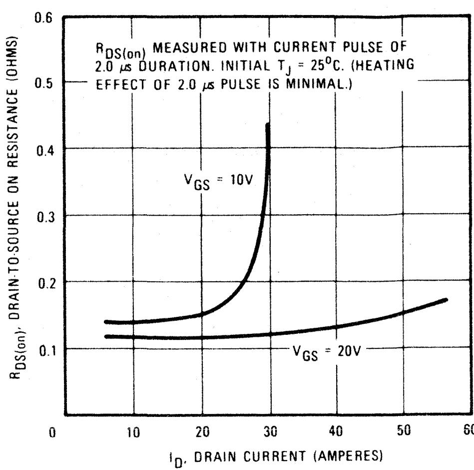


Fig. 12 — Typical On-Resistance Vs. Drain Current

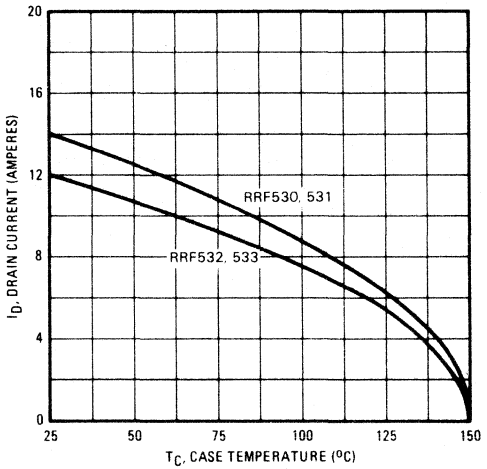


Fig. 13 — Maximum Drain Current Vs. Case Temperature

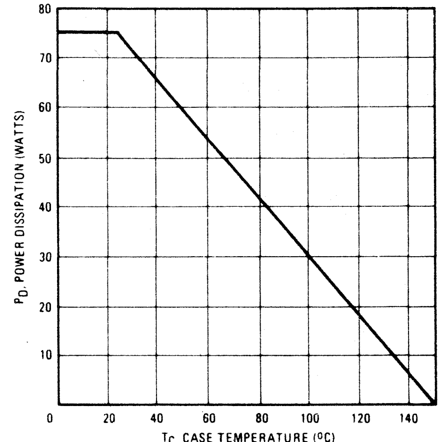


Fig. 14 — Power Vs. Temperature Derating Curve

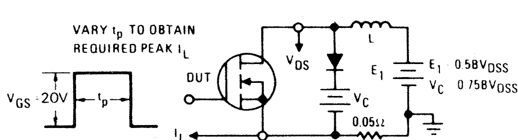


Fig. 15 — Clamped Inductive Test Circuit

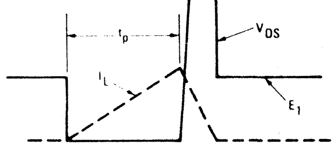


Fig. 16 — Clamped Inductive Waveforms

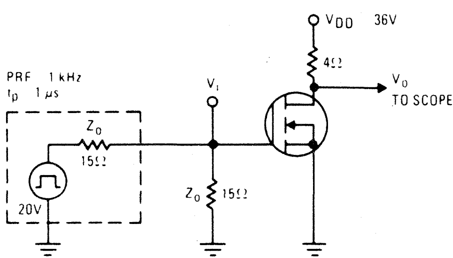


Fig. 17 — Switching Time Test Circuit

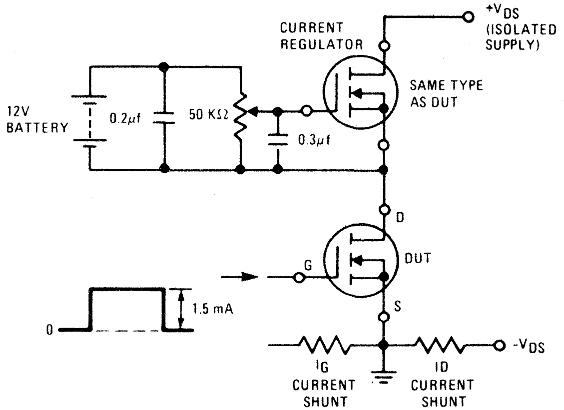


Fig. 18 — Gate Charge Test Circuit

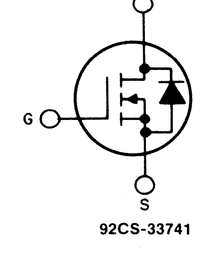
N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 150V-200V

$r_{DS}(on)$ = 1.5 Ω and 2.4 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



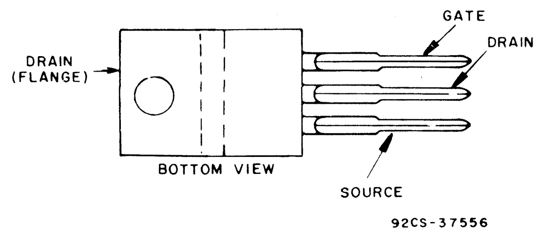
N-CHANNEL ENHANCEMENT MODE

The RRF610, RRF611, RRF612 and RRF613* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF610, IRF611, IRF612 and IRF613, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

Absolute Maximum Ratings

Parameter		RRF610	RRF611	RRF612	RRF613	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF610 RRF612	200	—	—	V	V_{GS} = 0V
		RRF611 RRF613	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF610 RRF611	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF612 RRF613	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF610 RRF611	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		RRF612 RRF613		1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

D, LD, G, LS, S

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF610 RRF611			2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF612 RRF613			2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF610 RRF611			10	A	
		RRF612 RRF613		—	8.0	A	
V_{SD}	Diode Forward Voltage ②	RRF610 RRF611			2.0	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		RRF612 RRF613			1.8	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL		290		ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0		μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				

D, G, S

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

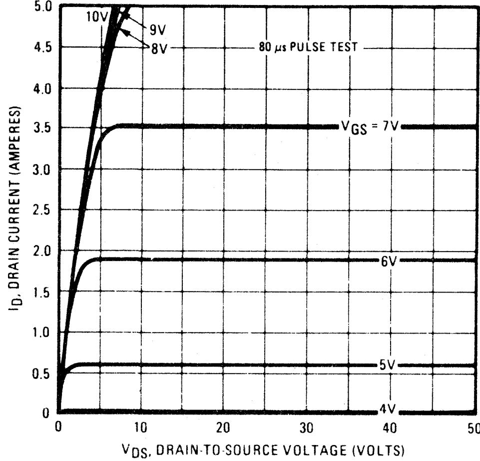


Fig. 1 — Typical Output Characteristics

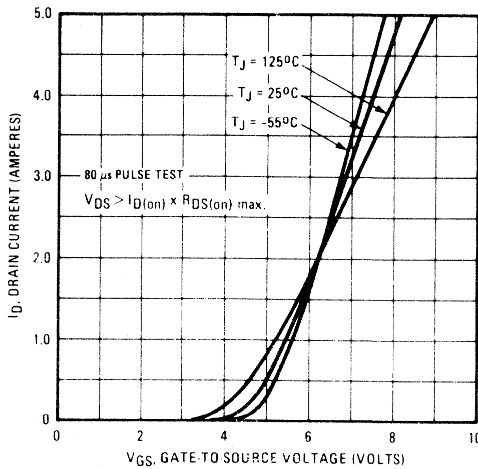


Fig. 2 — Typical Transfer Characteristics

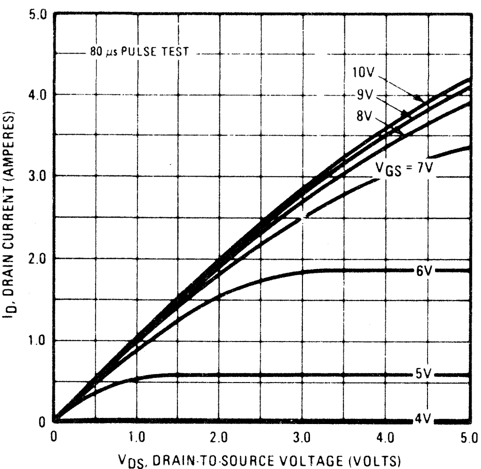


Fig. 3 — Typical Saturation Characteristics

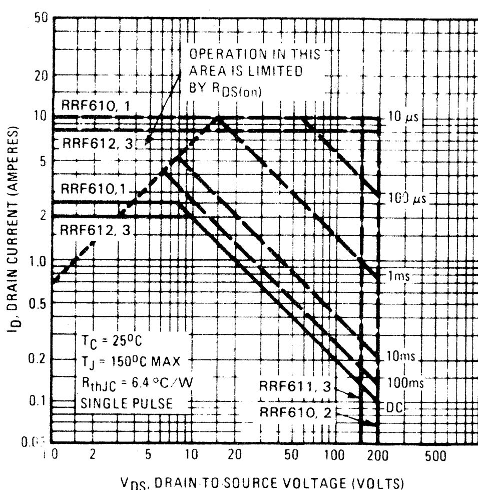


Fig. 4 — Maximum Safe Operating Area

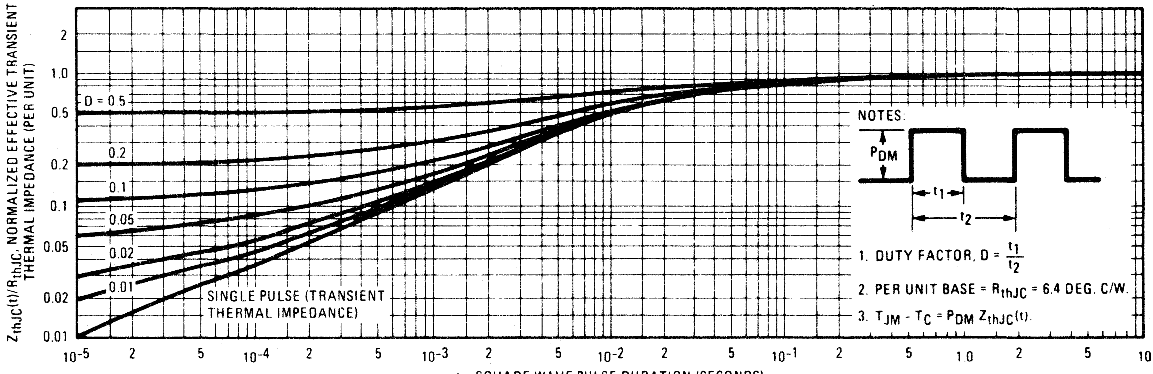


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

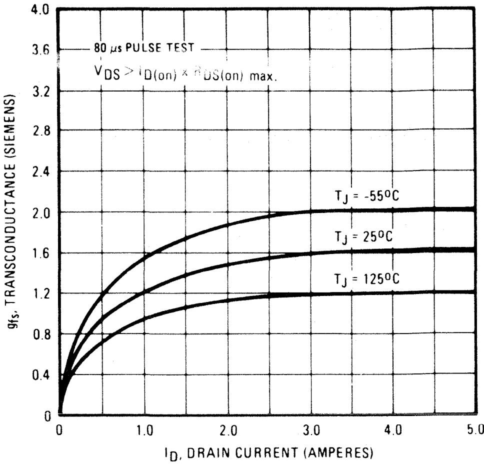


Fig. 6 — Typical Transconductance Vs. Drain Current

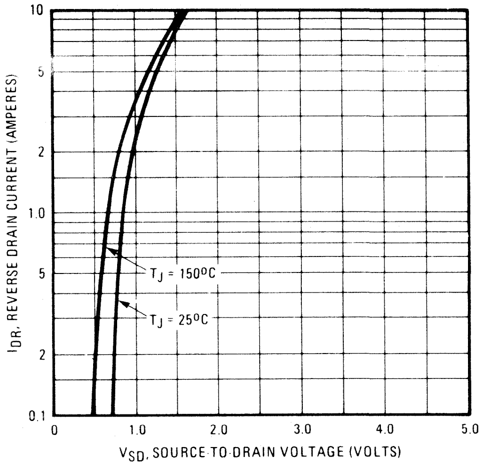


Fig. 7 — Typical Source-Drain Diode Forward Voltage

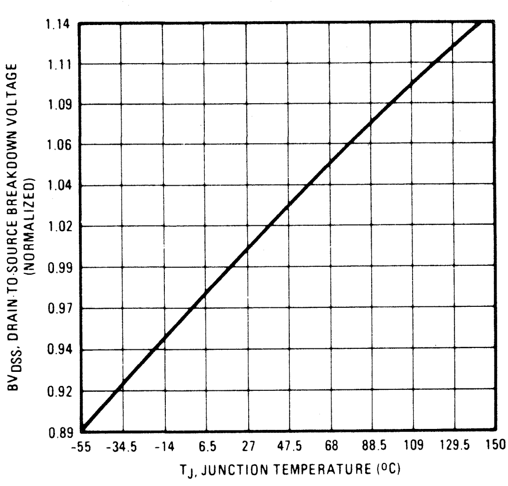


Fig. 8 — Breakdown Voltage Vs. Temperature

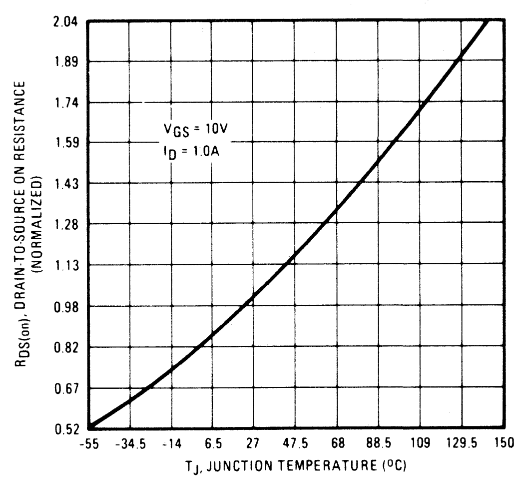


Fig. 9 — Normalized On-Resistance Vs. Temperature

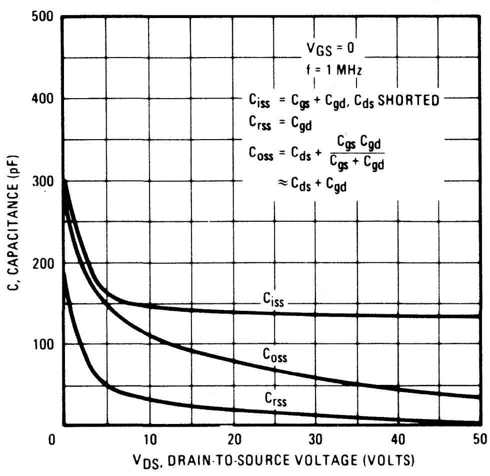


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

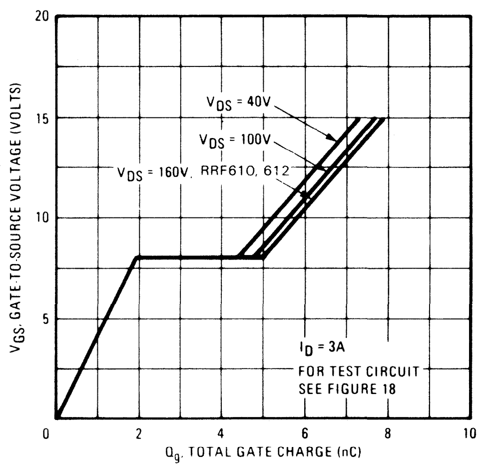


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

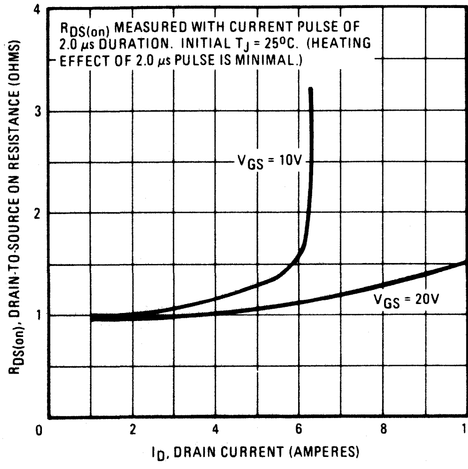


Fig. 12 — Typical On-Resistance Vs. Drain Current

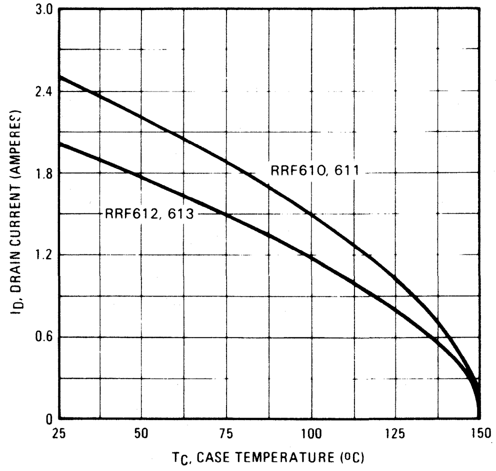


Fig. 13 — Maximum Drain Current Vs. Case Temperature

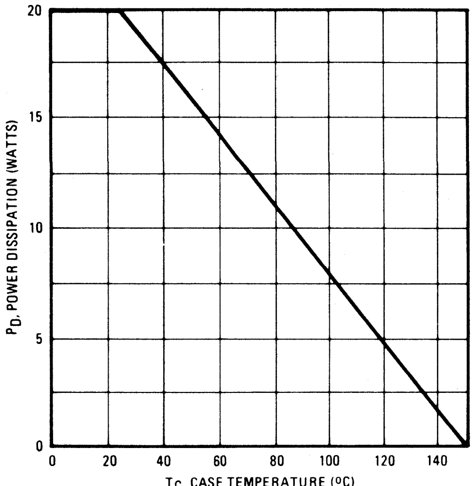


Fig. 14 — Power Vs. Temperature Derating Curve

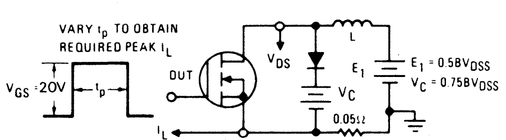


Fig. 15 — Clamped Inductive Test Circuit

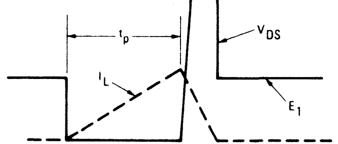


Fig. 16 — Clamped Inductive Waveforms

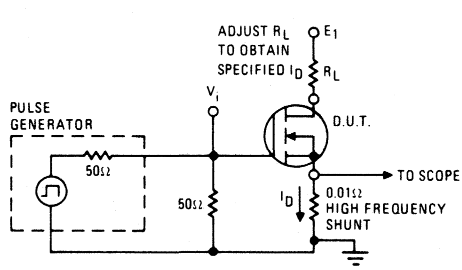


Fig. 17 — Switching Time Test Circuit

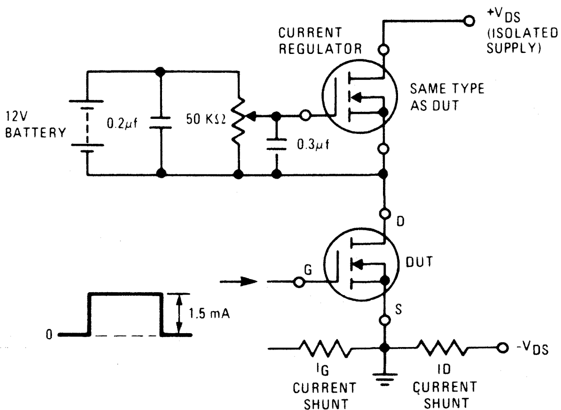


Fig. 18 — Gate Charge Test Circuit

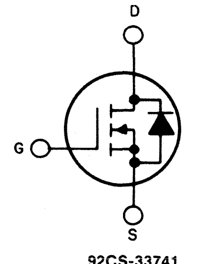
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

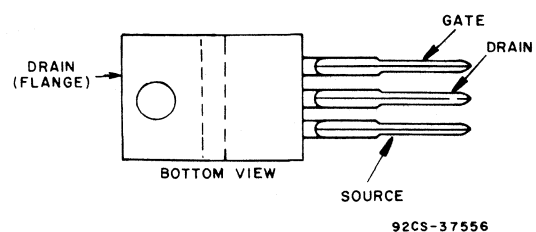


N-CHANNEL ENHANCEMENT MODE

The RRF620, RRF621, RRF622 and RRF623* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

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*These devices are equivalent to International Rectifier Power MOSFETs IRF620, IRF621, IRF622 and IRF623, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF620	RRF621	RRF622	RRF623	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	20	20	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

RRF620, RRF621, RRF622, RRF623

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF620 RRF622	200	–	–	V	V_{GS} = 0V
		RRF621 RRF623	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL		–	500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF620 RRF621	5.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		RRF622 RRF623	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF620 RRF621	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		RRF622 RRF623	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 50V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF620 RRF621	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF622 RRF623	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF620 RRF621	–	–	20	A	
		RRF622 RRF623	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	RRF620 RRF621	–	–	1.8	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		RRF622 RRF623	–	–	1.4	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

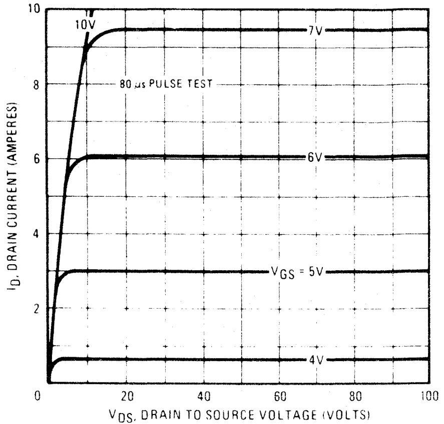


Fig. 1 — Typical Output Characteristics

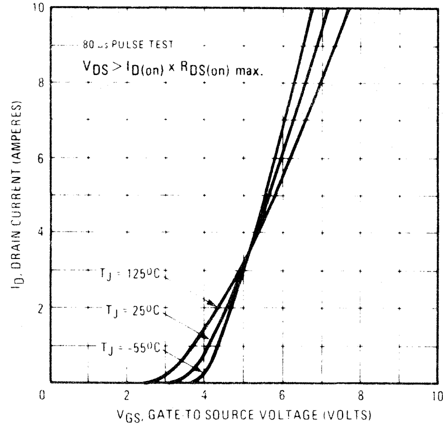


Fig. 2 — Typical Transfer Characteristics

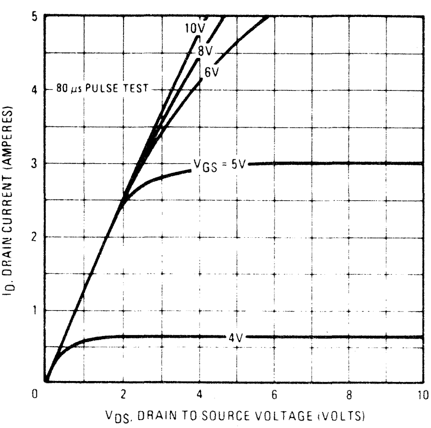


Fig. 3 — Typical Saturation Characteristics

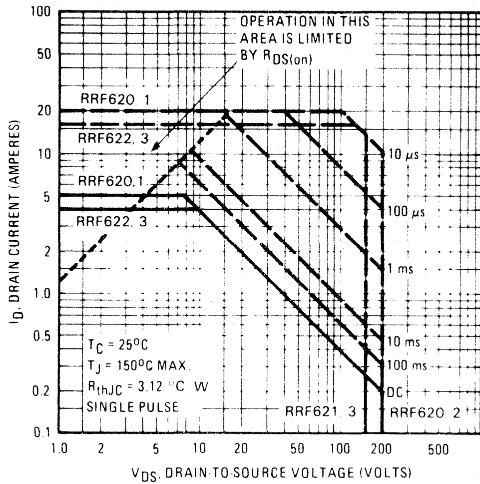


Fig. 4 — Maximum Safe Operating Area

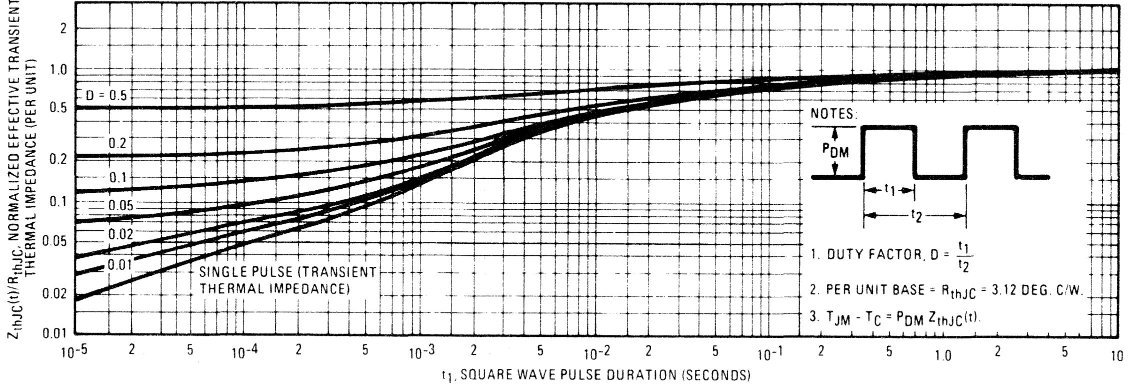


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

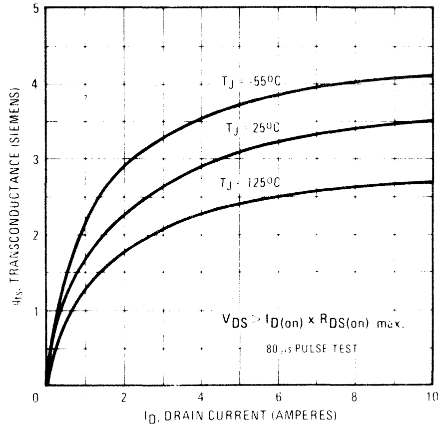


Fig. 6 — Typical Transconductance Vs. Drain Current

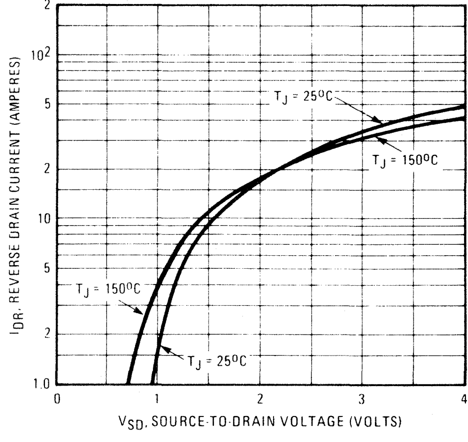


Fig. 7 — Typical Source-Drain Diode Forward Voltage

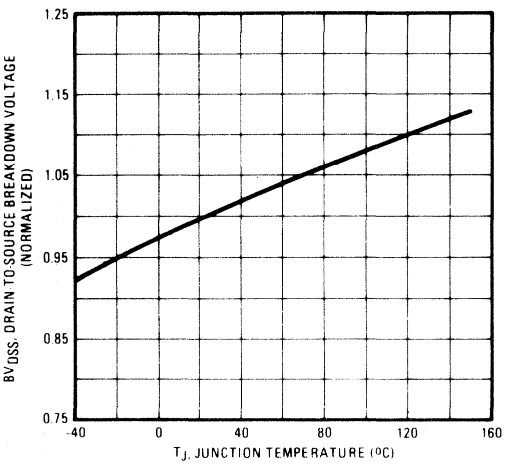


Fig. 8 — Breakdown Voltage Vs. Temperature

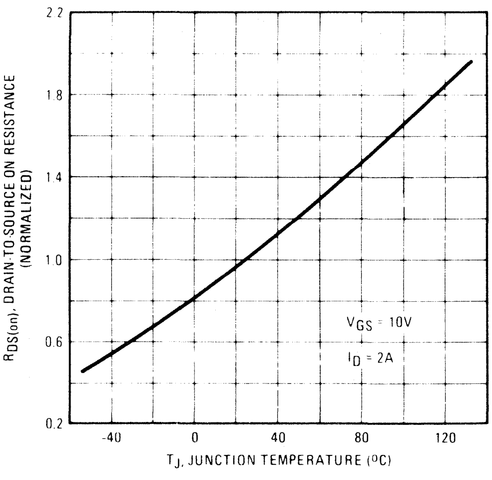


Fig. 9 — Normalized On-Resistance Vs. Temperature

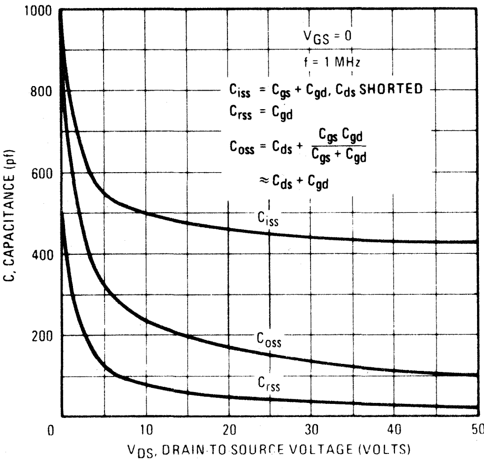


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

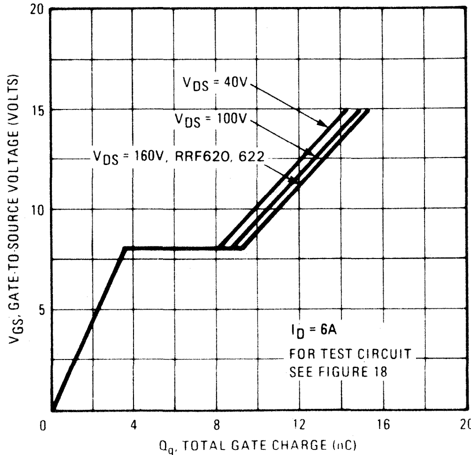


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

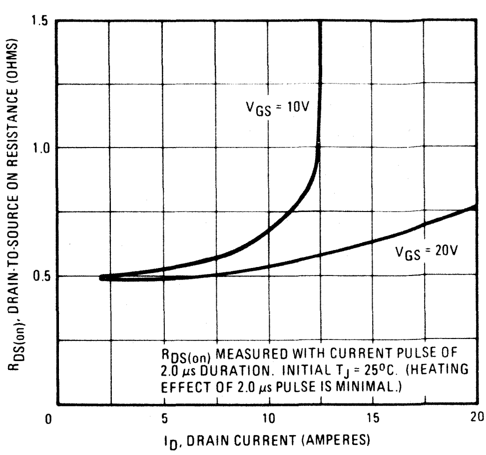


Fig. 12 — Typical On-Resistance Vs. Drain Current

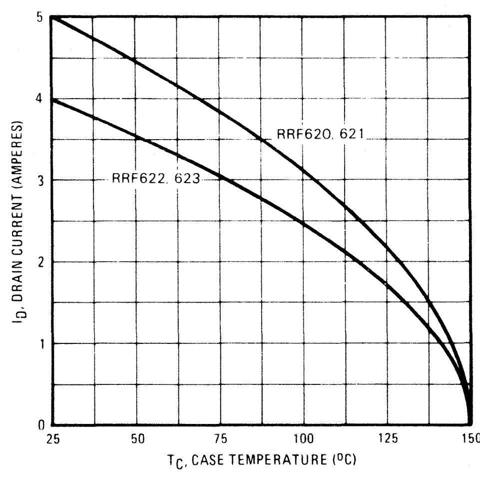


Fig. 13 — Maximum Drain Current Vs. Case Temperature

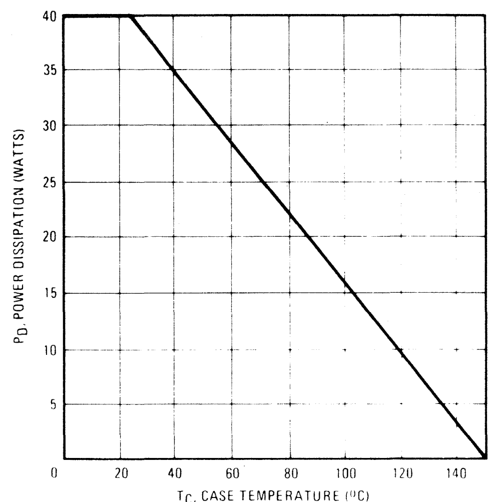


Fig. 14 — Power Vs. Temperature Derating Curve

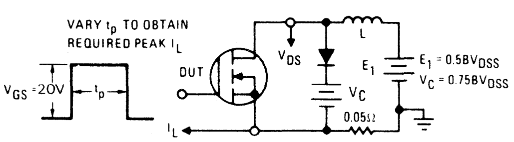


Fig. 15 — Clamped Inductive Test Circuit

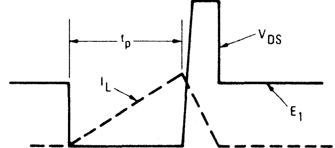


Fig. 16 — Clamped Inductive Waveforms

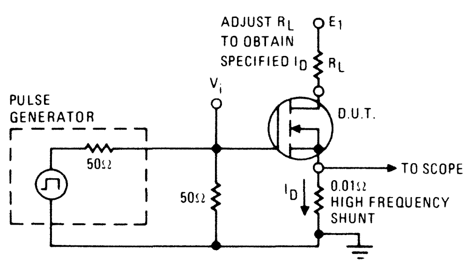


Fig. 17 — Switching Time Test Circuit

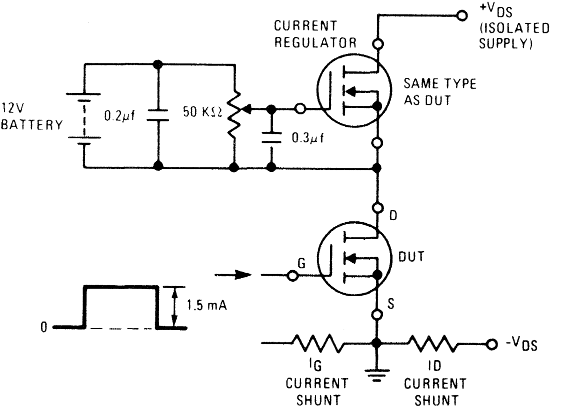


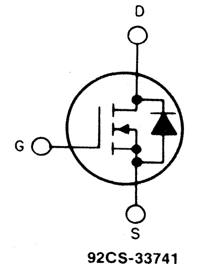
Fig. 18 — Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



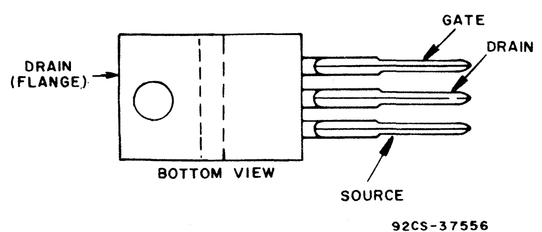
N-CHANNEL ENHANCEMENT MODE

The RRF630, RRF631, RRF632 and RRF633* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF630, IRF631, IRF632 and IRF633, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

Absolute Maximum Ratings

	Parameter	RRF630	RRF631	RRF632	RRF633	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	36	36	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF630 RRF632	200	–	–	V	V_{GS} = 0V
		RRF631 RRF633	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF630 RRF631	9.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		RRF632 RRF633	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF630 RRF631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		RRF632 RRF633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8		S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF630 RRF631	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF632 RRF633	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF630 RRF631	–	–	36	A	
		RRF632 RRF633	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	RRF630 RRF631	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		RRF632 RRF633	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

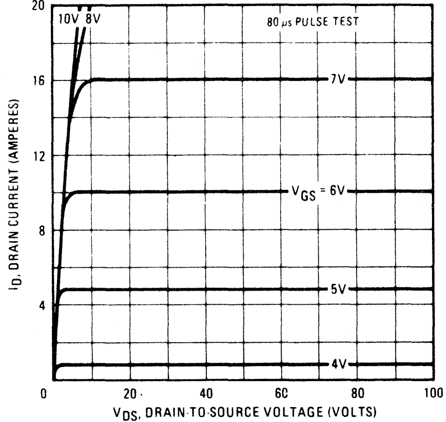


Fig. 1 — Typical Output Characteristics

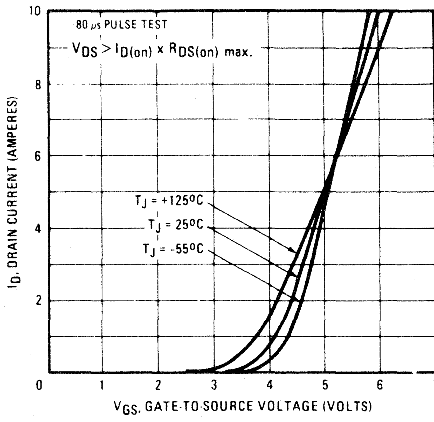


Fig. 2 — Typical Transfer Characteristics

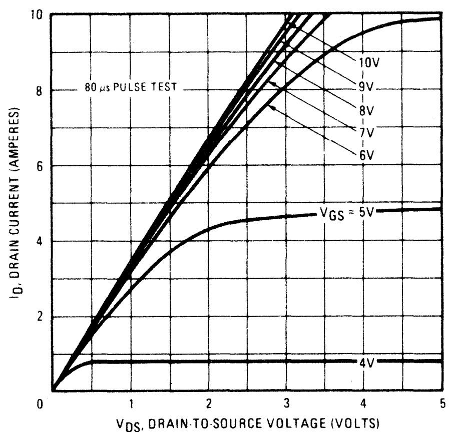


Fig. 3 — Typical Saturation Characteristics

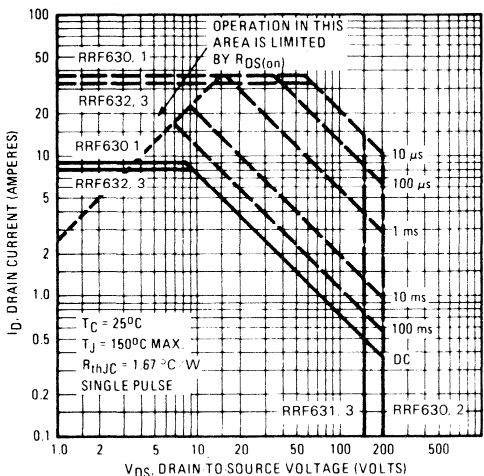


Fig. 4 — Maximum Safe Operating Area

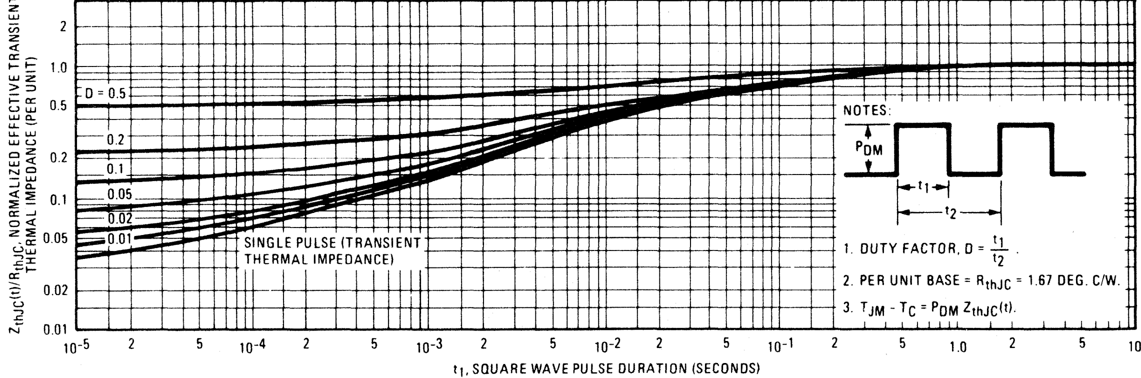


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

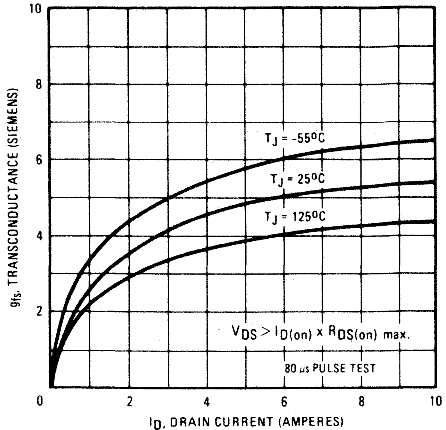


Fig. 6 — Typical Transconductance Vs. Drain Current

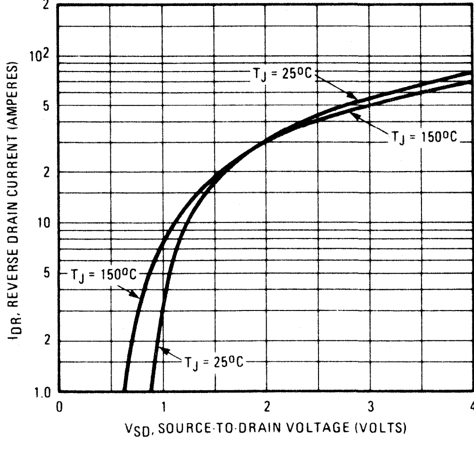


Fig. 7 — Typical Source-Drain Diode Forward Voltage

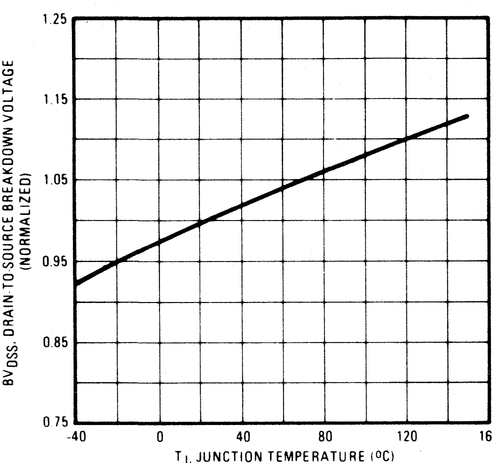


Fig. 8 — Breakdown Voltage Vs. Temperature

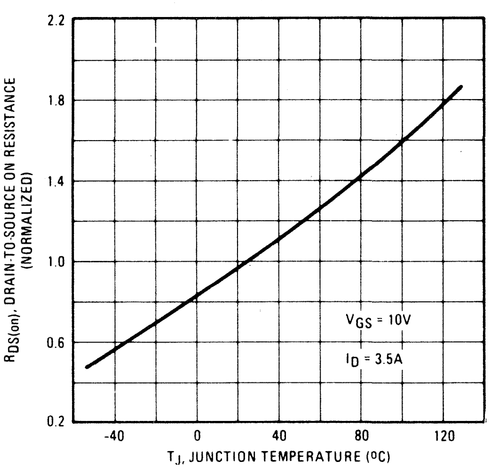


Fig. 9 — Normalized On-Resistance Vs. Temperature

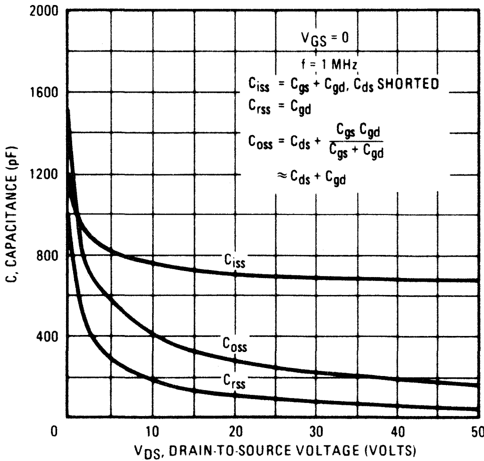


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

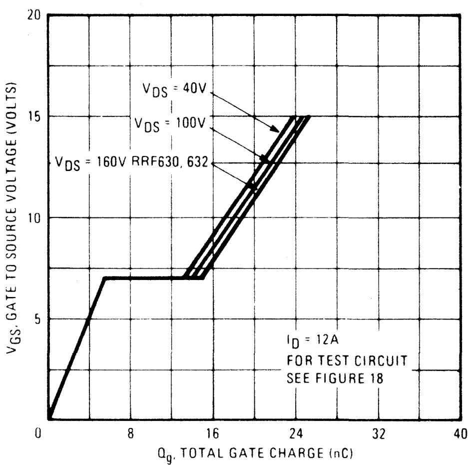


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

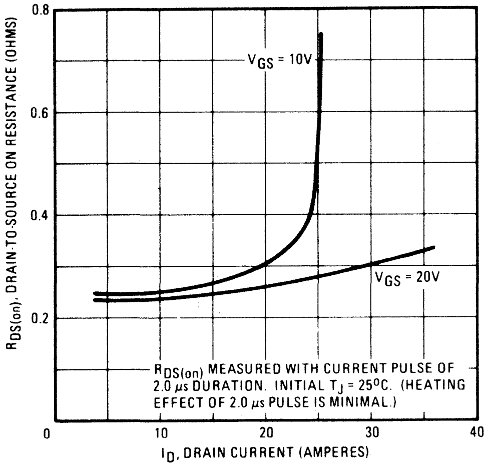


Fig. 12 – Typical On-Resistance Vs. Drain Current

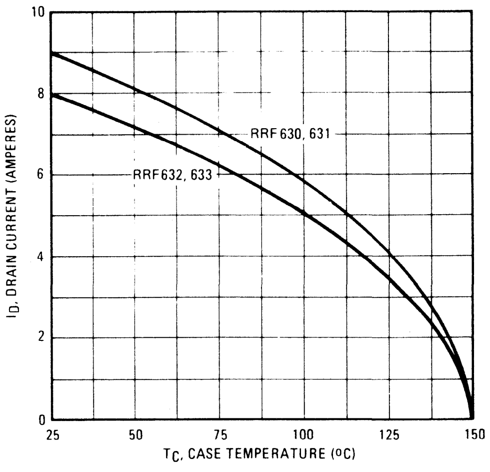


Fig. 13 – Maximum Drain Current Vs. Case Temperature

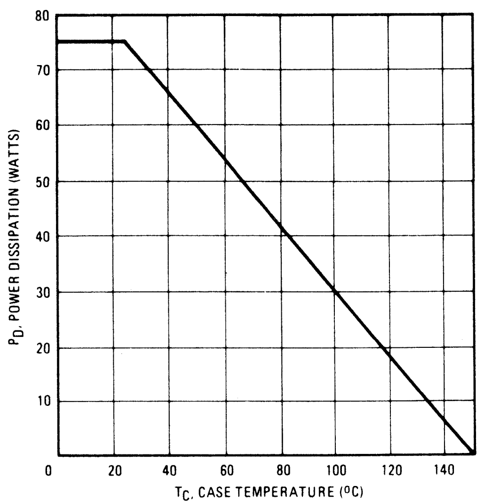


Fig. 14 – Power Vs. Temperature Derating Curve

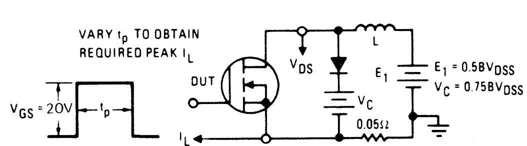


Fig. 15 – Clamped Inductive Test Circuit

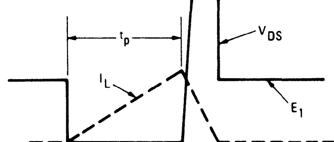


Fig. 16 – Clamped Inductive Waveforms

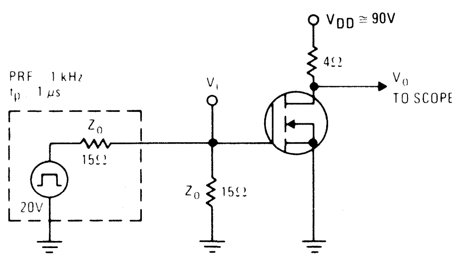


Fig. 17 – Switching Time Test Circuit

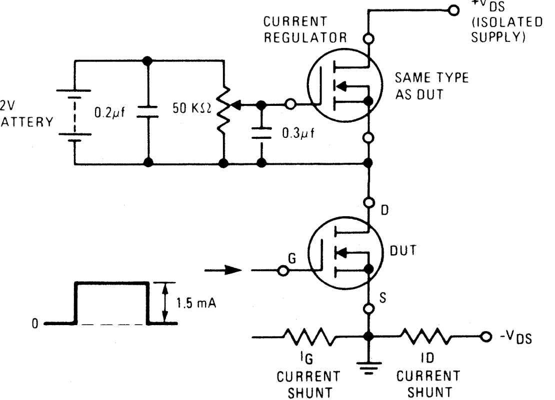


Fig. 18 – Gate Charge Test Circuit

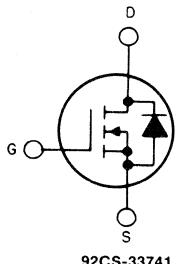
N-Channel Enhancement-Mode Power Field-Effect Transistors

16A and 18A, 150V

$r_{DS}(on)$ = 0.18 Ω and 0.22 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

N-CHANNEL ENHANCEMENT MODE

The RRF641 and RRF643* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

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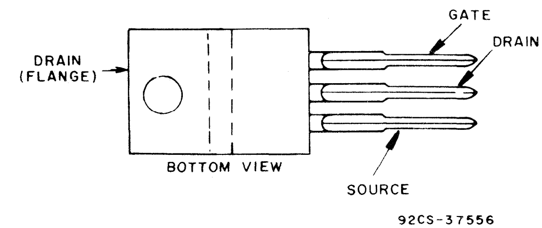
*These devices are equivalent to International Rectifier Power MOSFETs IRF641 and IRF643, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



92CS-37556

JEDEC TO-220AB

Absolute Maximum Ratings

Parameter		RRF641	RRF643	Units
V_{DS}	Drain - Source Voltage ①	150	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	150	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	10	A
I_{DM}	Pulsed Drain Current ③	72	64	A
V_{GS}	Gate - Source Voltage	± 20		V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)		W
	Linear Derating Factor	1.0 (See Fig. 14)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 72 | 72 | 64 | 64		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 100		°C
	Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF641 RRF643	150	—	—	V	V_{GS} = 0V I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF641	18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF643	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF641	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		RRF643	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	V_{DD} = 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	
t_f	Fall Time	ALL	—	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF641	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF643	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF641	—	—	72	A	
		RRF643	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	RRF641	—	—	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		RRF643	—	—	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

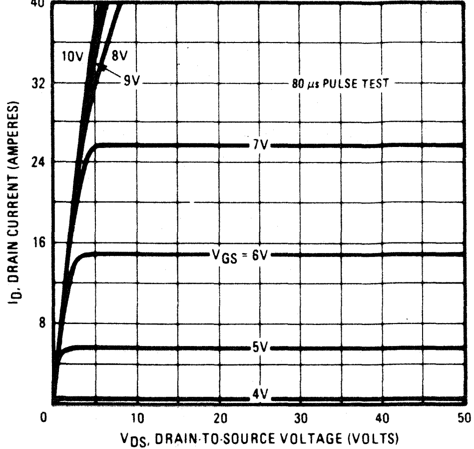


Fig. 1 — Typical Output Characteristics

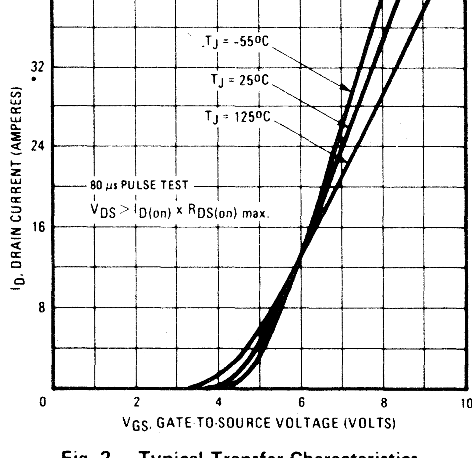


Fig. 2 — Typical Transfer Characteristics

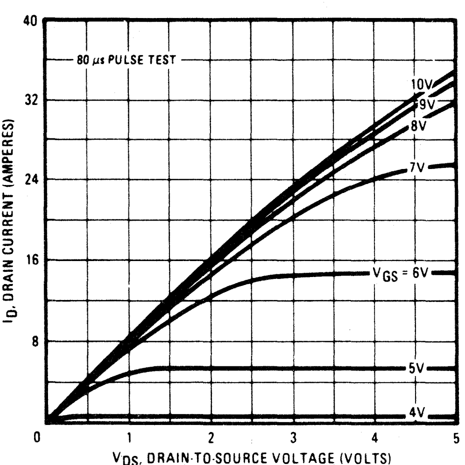


Fig. 3 — Typical Saturation Characteristics

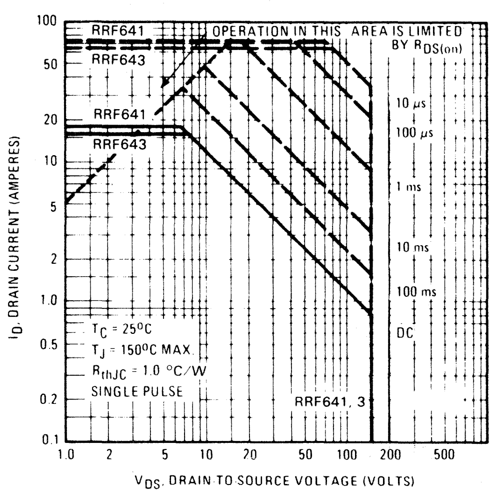


Fig. 4 — Maximum Safe Operating Area

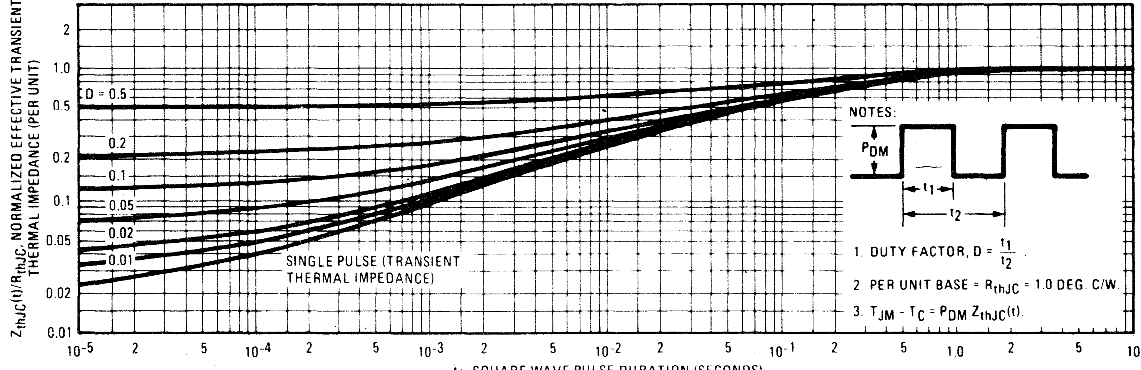


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

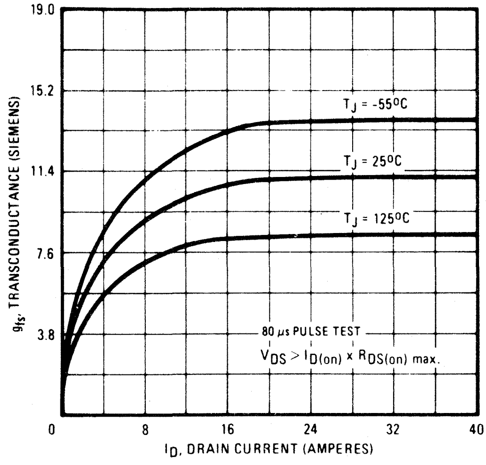


Fig. 6 — Typical Transconductance Vs. Drain Current

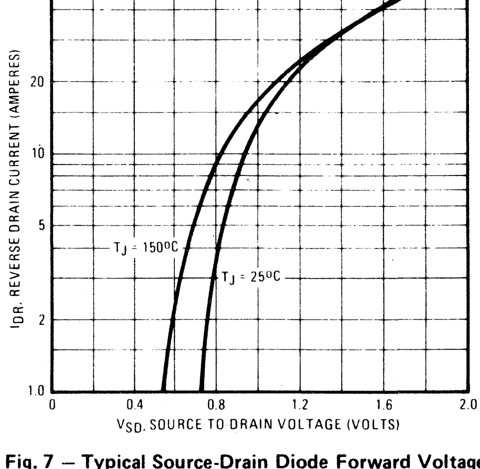


Fig. 7 — Typical Source-Drain Diode Forward Voltage

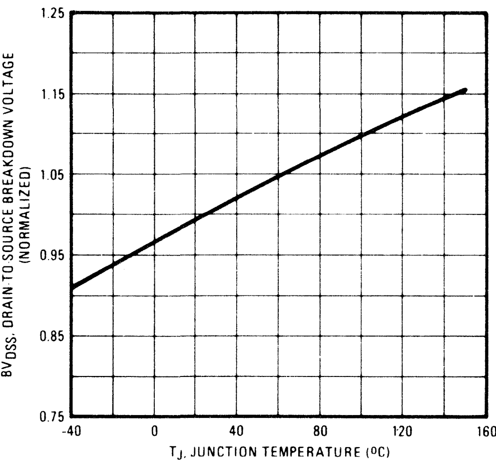


Fig. 8 — Breakdown Voltage Vs. Temperature

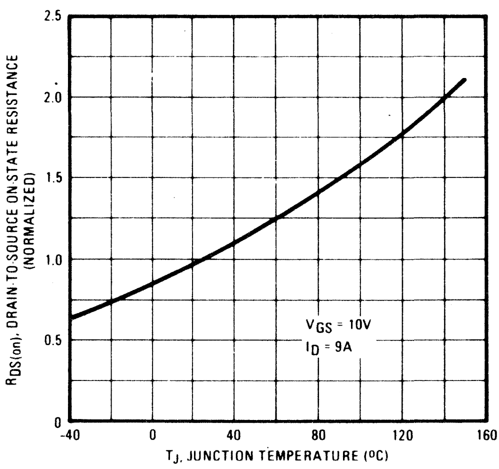


Fig. 9 — Normalized On-Resistance Vs. Temperature

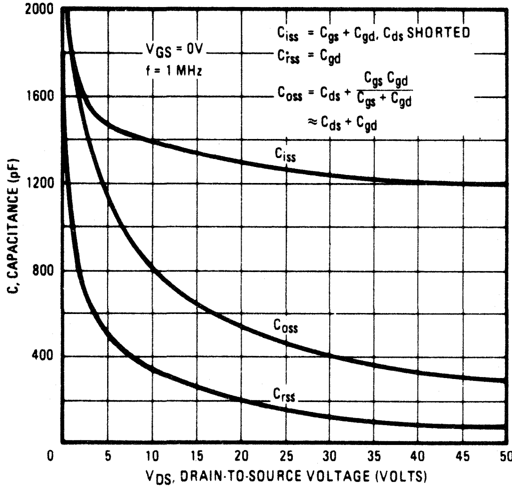


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

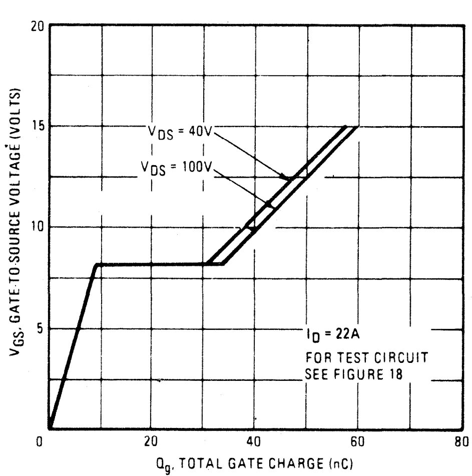


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

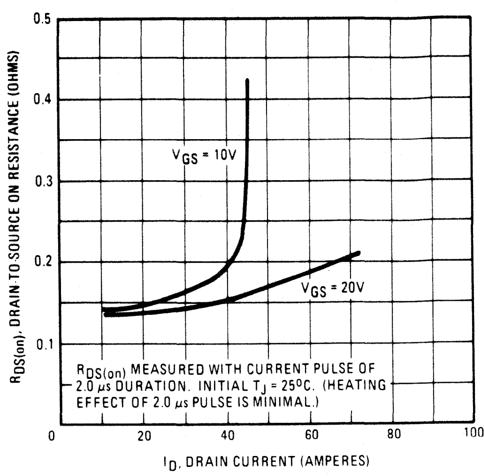


Fig. 12 — Typical On-Resistance Vs. Drain Current

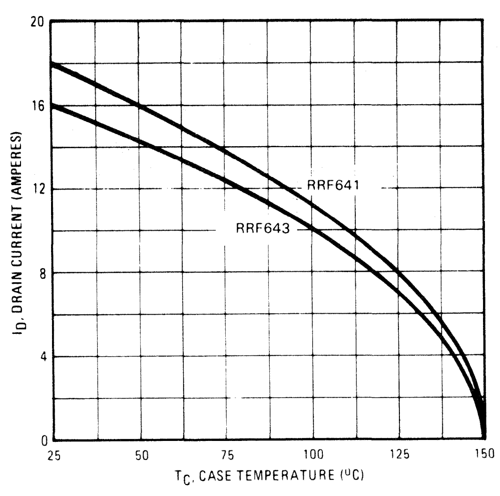


Fig. 13 — Maximum Drain Current Vs. Case Temperature

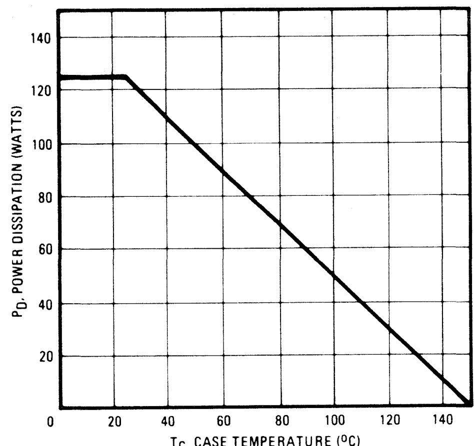


Fig. 14 — Power Vs. Temperature Derating Curve

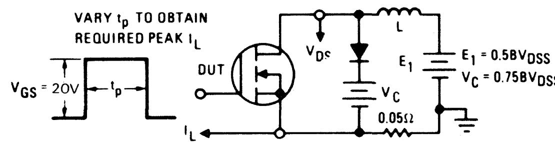


Fig. 15 — Clamped Inductive Test Circuit

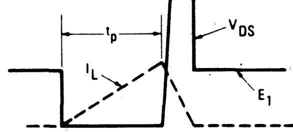


Fig. 16 — Clamped Inductive Waveforms

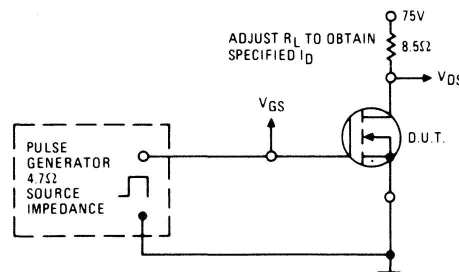


Fig. 17 — Switching Time Test Circuit

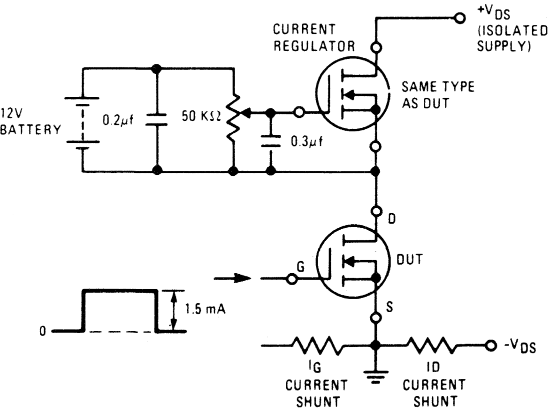


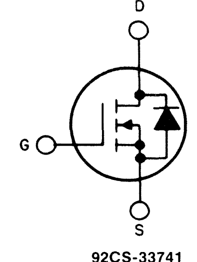
Fig. 18 — Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

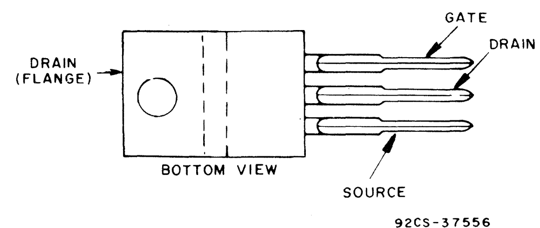
N-CHANNEL ENHANCEMENT MODE

The RRF720, RRF721, RRF722 and RRF723* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF720, IRF721, IRF722 and IRF723, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



92CS-37556

JEDEC TO-220AB

Absolute Maximum Ratings

	Parameter	RRF720	RRF721	RRF722	RRF723	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 12	12	10	10	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	RRF720 RRF722	400	–	–	V	V_{GS} = 0V
	RRF721 RRF723	350	–	–	V	I_D = 250μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS} Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ②	RRF720 RRF721	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
	RRF722 RRF723	2.5	–	–	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	RRF720 RRF721	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
	RRF722 RRF723	–	1.8	2.5	Ω	
g_{fs} Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss} Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	–	100	200	pF	
C_{rss} Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	–	50	100	ns	
t_f Fall Time	ALL	–	25	50	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
		–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

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Thermal Resistance

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC} Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS} Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	RRF720 RRF721	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	RRF722 RRF723	–	–	2.5	A	
I_{SM} Pulse Source Current (Body Diode) ③	RRF720 RRF721	–	–	12	A	
	RRF722 RRF723	–	–	10	A	
V_{SD} Diode Forward Voltage ②	RRF720 RRF721	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
	RRF722 RRF723	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr} Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
Q_{RR} Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

D G S

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

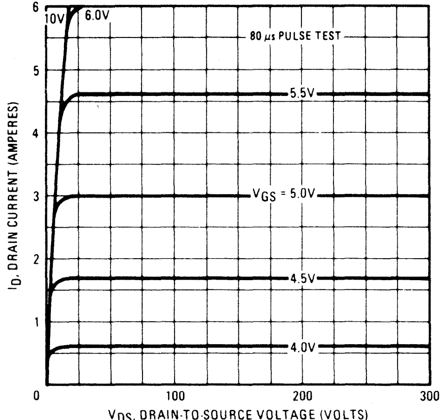


Fig. 1 — Typical Output Characteristics

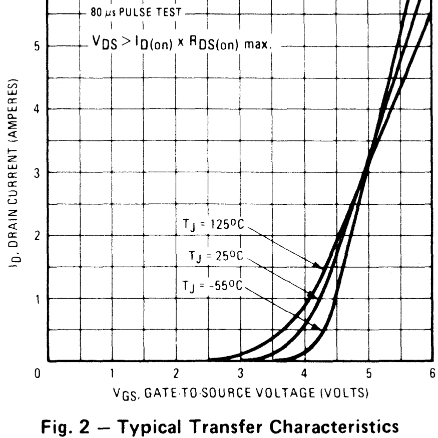


Fig. 2 — Typical Transfer Characteristics

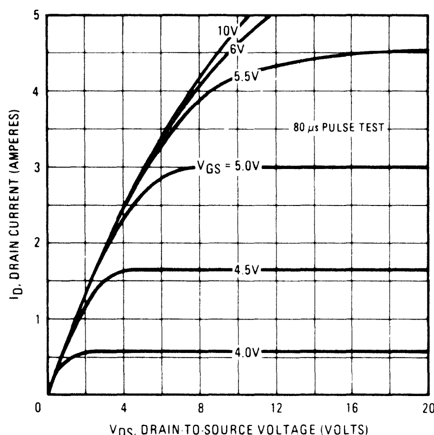


Fig. 3 — Typical Saturation Characteristics

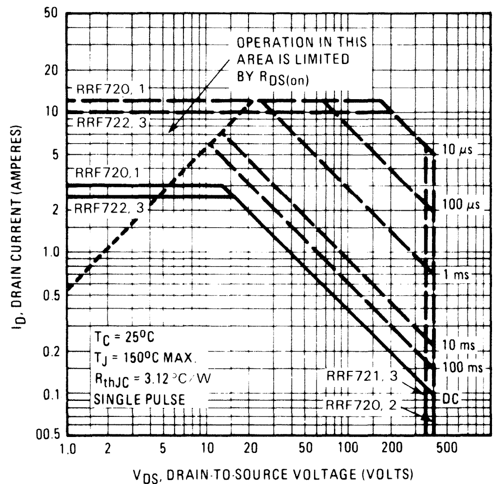


Fig. 4 — Maximum Safe Operating Area

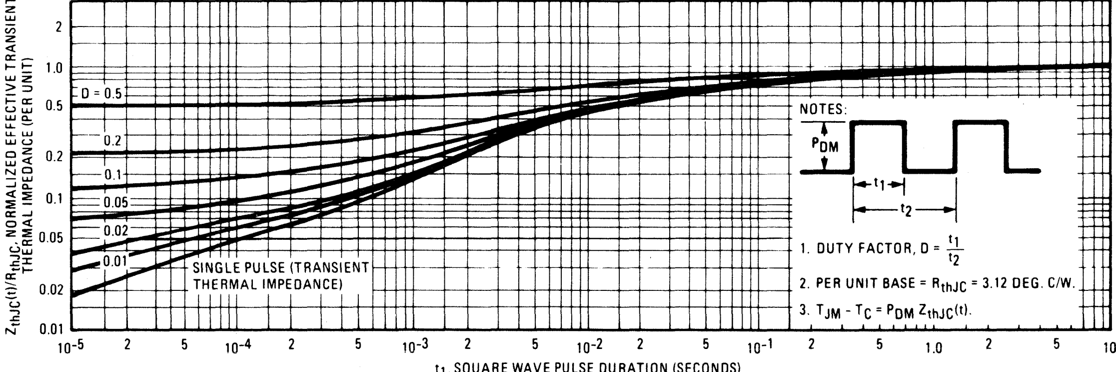


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

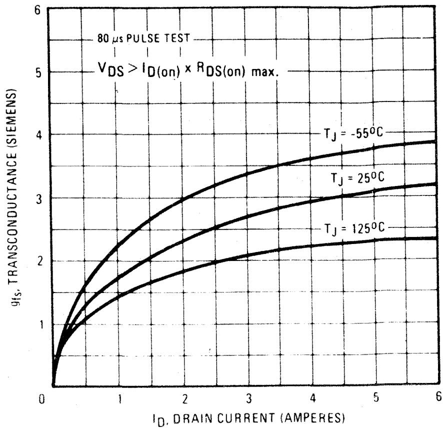


Fig. 6 — Typical Transconductance Vs. Drain Current

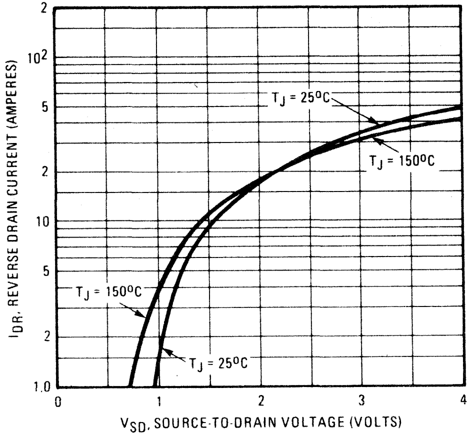


Fig. 7 — Typical Source-Drain Diode Forward Voltage

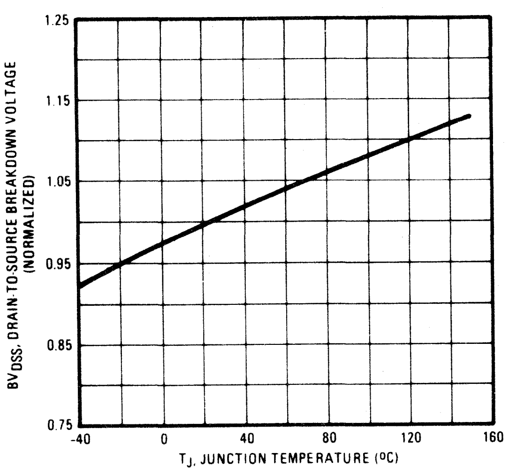


Fig. 8 — Breakdown Voltage Vs. Temperature

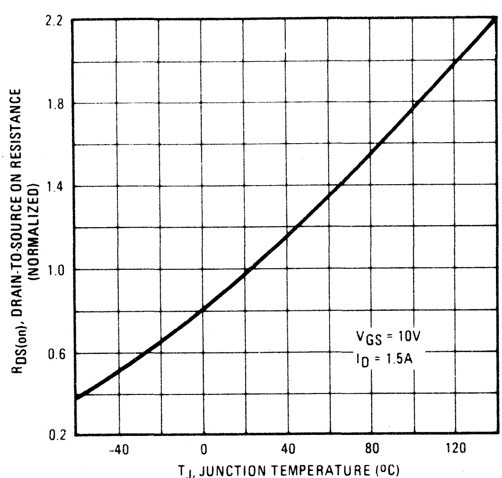


Fig. 9 — Normalized On-Resistance Vs. Temperature

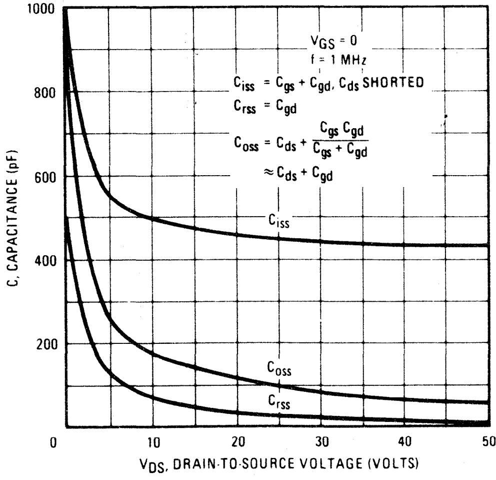


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

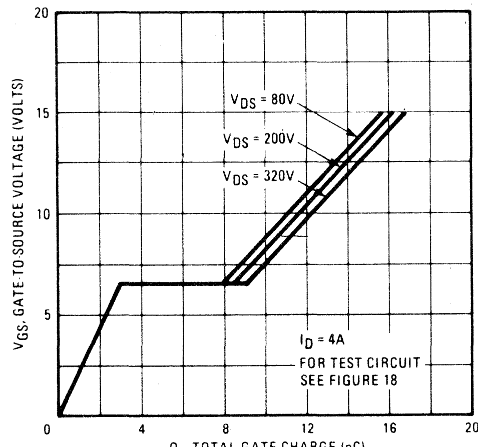


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

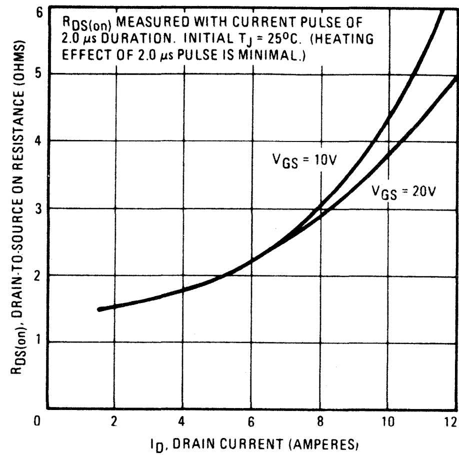


Fig. 12 – Typical On-Resistance Vs. Drain Current

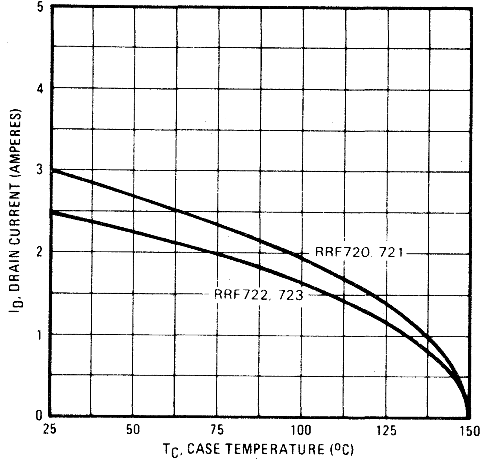


Fig. 13 – Maximum Drain Current Vs. Case Temperature

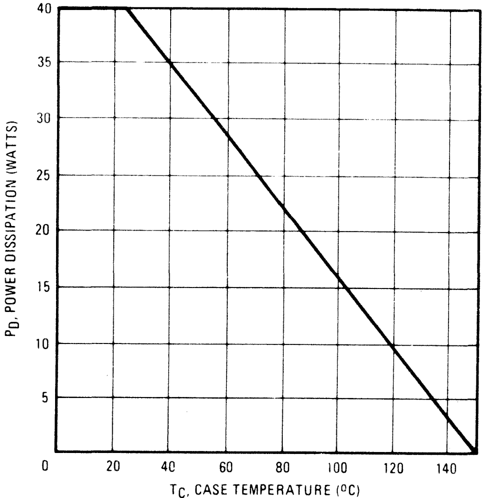


Fig. 14 – Power Vs. Temperature Derating Curve

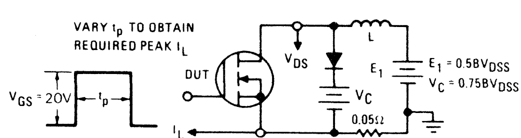


Fig. 15 – Clamped Inductive Test Circuit

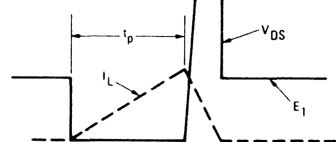


Fig. 16 – Clamped Inductive Waveforms

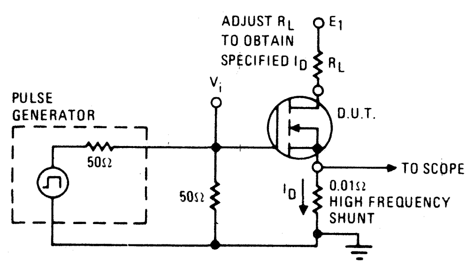


Fig. 17 – Switching Time Test Circuit

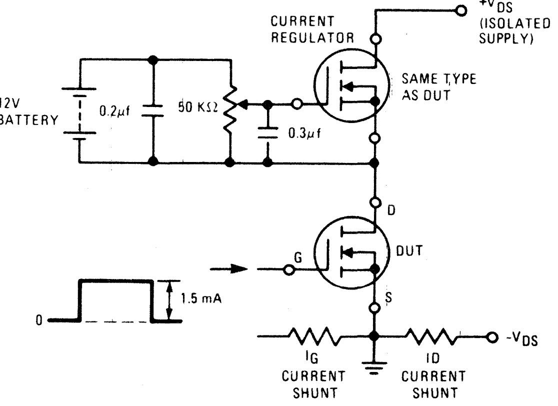


Fig. 18 – Gate Charge Test Circuit

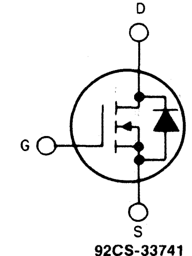
RRF730, RRF731, RRF732, RRF733 *

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

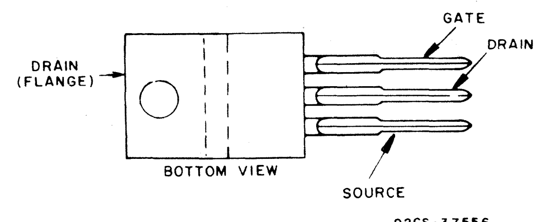
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



92CS-37556

JEDEC TO-220AB

The RRF730, RRF731, RRF732 and RRF733* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF730, IRF731, IRF732 and IRF733, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF730	RRF731	RRF732	RRF733	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 22	22	18	18	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

RRF730, RRF731, RRF732, RRF733

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF730 RRF732	400	–	–	V	V_{GS} = 0V
		RRF731 RRF733	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF730 RRF731	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		RRF732 RRF733	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF730 RRF731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		RRF732 RRF733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

D
LD
G
LS
S

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF730 RRF731	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF732 RRF733	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF730 RRF731	–	–	22	A	
		RRF732 RRF733	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	RRF730 RRF731	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		RRF732 RRF733	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

D
G
S

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

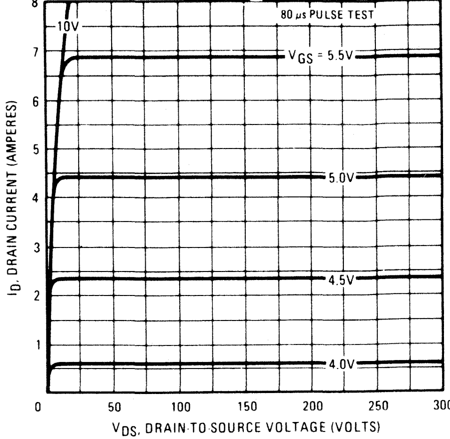


Fig. 1 — Typical Output Characteristics

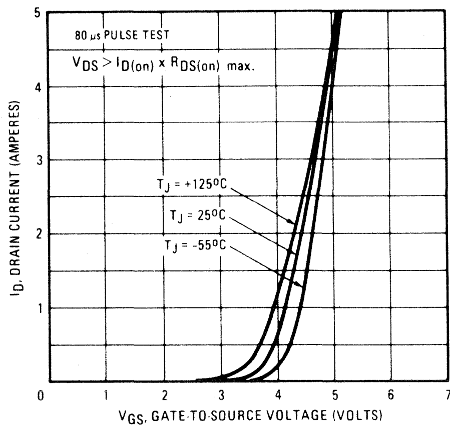


Fig. 2 — Typical Transfer Characteristics

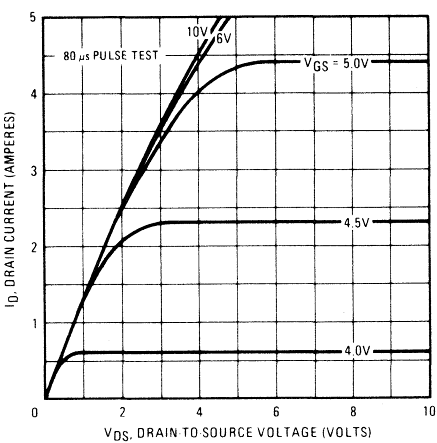


Fig. 3 — Typical Saturation Characteristics

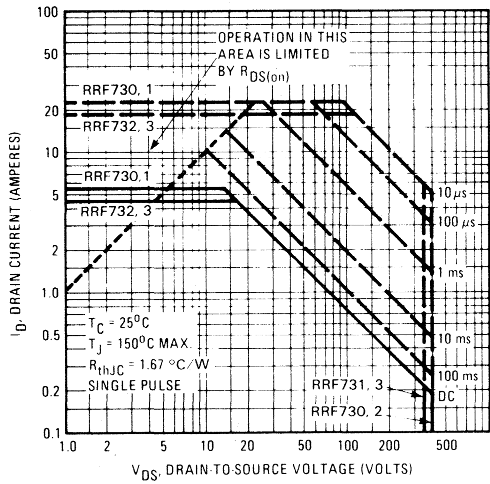


Fig. 4 — Maximum Safe Operating Area

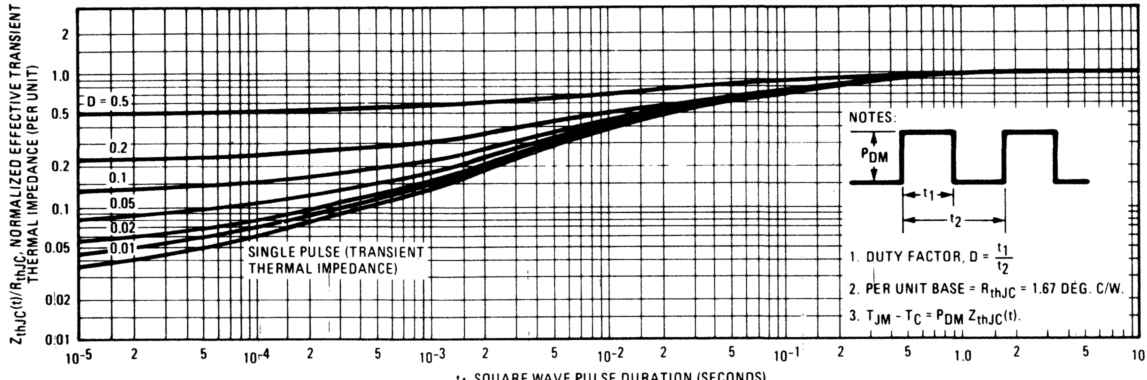


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

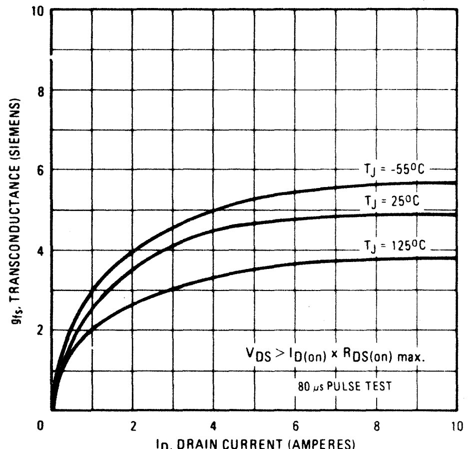


Fig. 6 — Typical Transconductance Vs. Drain Current

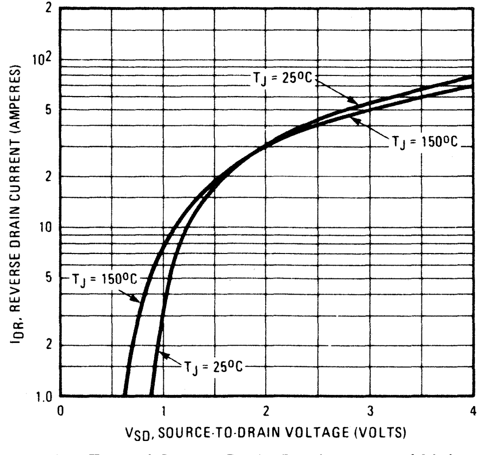


Fig. 7 — Typical Source-Drain Diode Forward Voltage

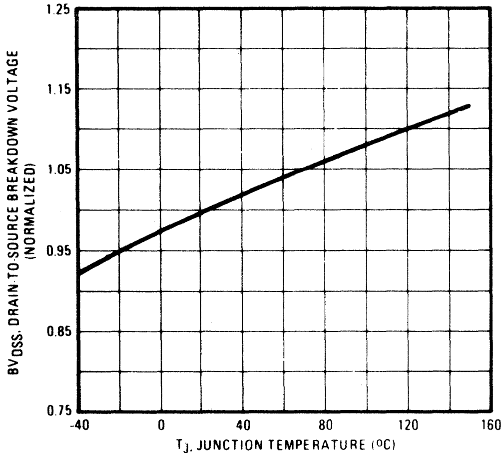


Fig. 8 — Breakdown Voltage Vs. Temperature

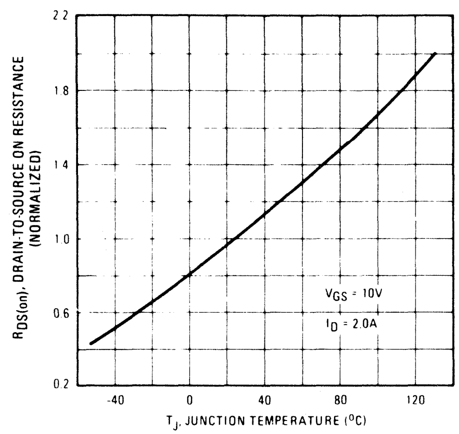


Fig. 9 — Normalized On-Resistance Vs. Temperature

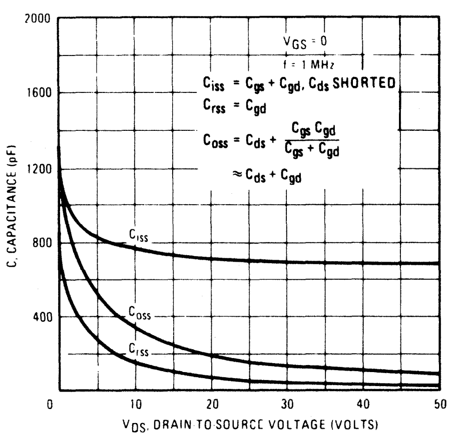


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

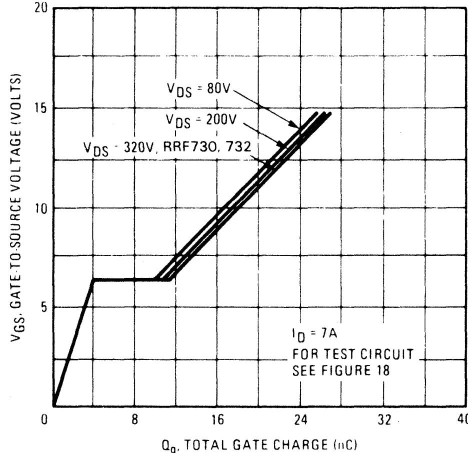


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

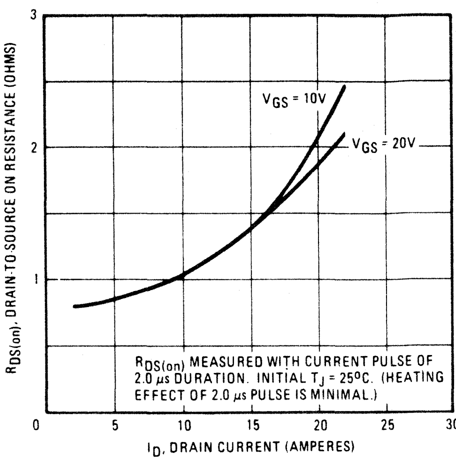


Fig. 12 — Typical On-Resistance Vs. Drain Current

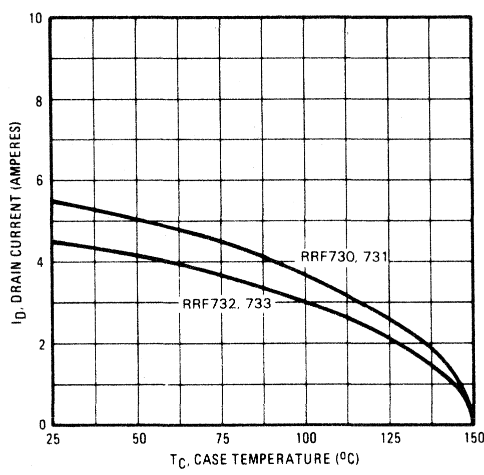


Fig. 13 — Maximum Drain Current Vs. Case Temperature

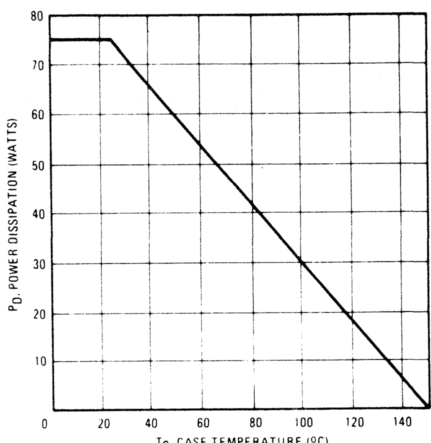


Fig. 14 — Power Vs. Temperature Derating Curve

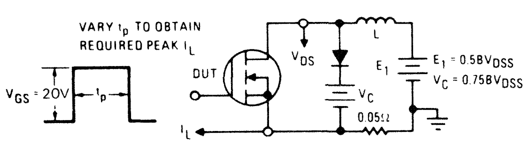


Fig. 15 — Clamped Inductive Test Circuit

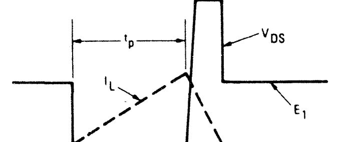


Fig. 16 — Clamped Inductive Waveforms

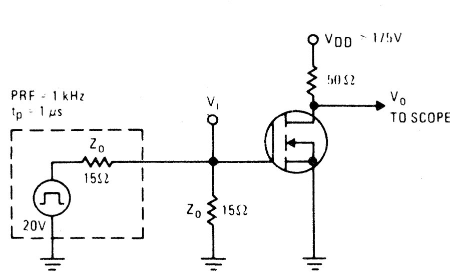


Fig. 17 — Switching Time Test Circuit

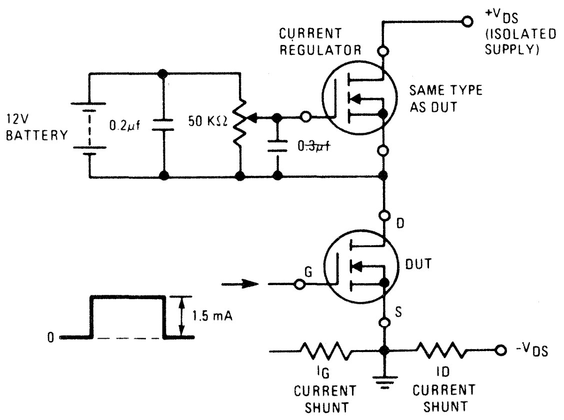


Fig. 18 — Gate Charge Test Circuit

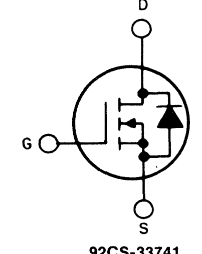
N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

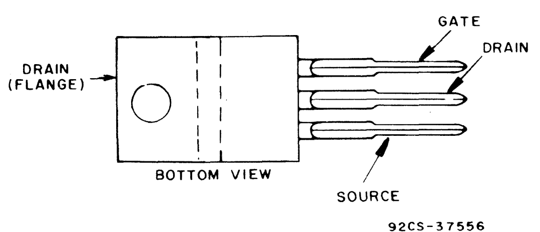
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-220AB

The RRF820, RRF821, RRF822 and RRF823* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

*These devices are equivalent to International Rectifier Power MOSFETs IRF820, IRF821, IRF822 and IRF823, and may be used as replacements therefore.

Absolute Maximum Ratings

	Parameter	RRF820	RRF821	RRF822	RRF823	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF820 RRF822	500	–	–	V	V_{GS} = 0V
		RRF821 RRF823	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF820 RRF821	2.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		RRF822 RRF823	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF820 RRF821	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		RRF822 RRF823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. — Modified MOSFET symbol showing the internal device inductances. (D, LD, G, LS, S)
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	RRF820 RRF821	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
		RRF822 RRF823	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF820 RRF821	–	–	10	A	
		RRF822 RRF823	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	RRF820 RRF821	–	–	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		RRF822 RRF823	–	–	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

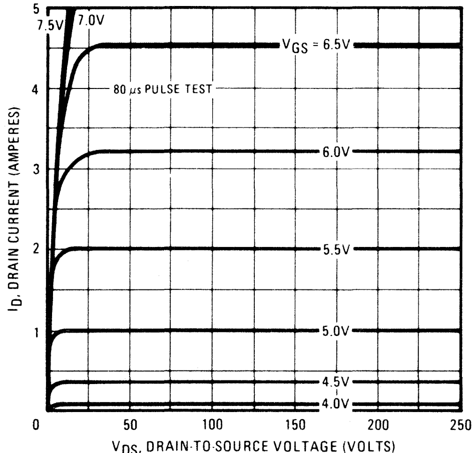


Fig. 1 — Typical Output Characteristics

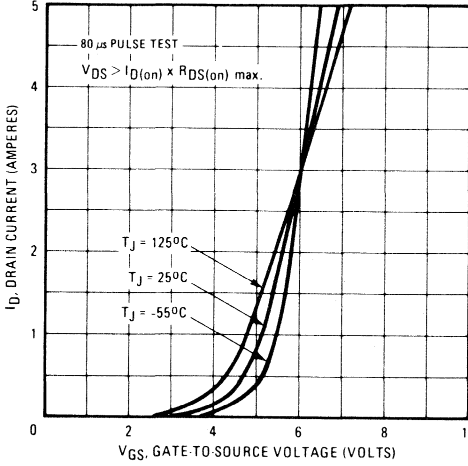


Fig. 2 — Typical Transfer Characteristics

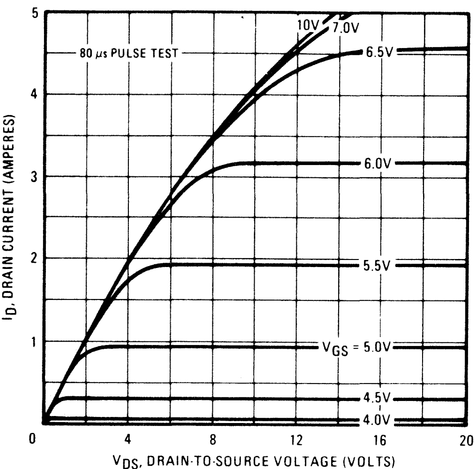


Fig. 3 — Typical Saturation Characteristics

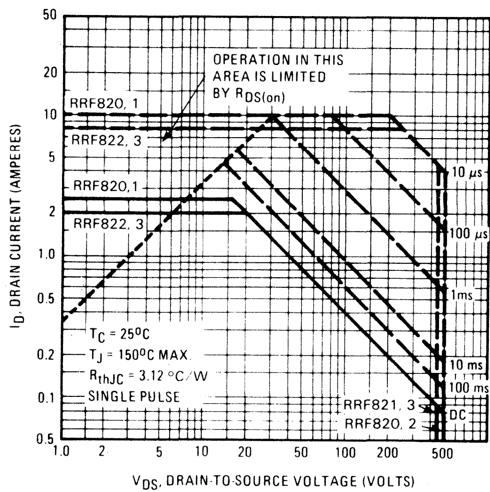


Fig. 4 — Maximum Safe Operating Area

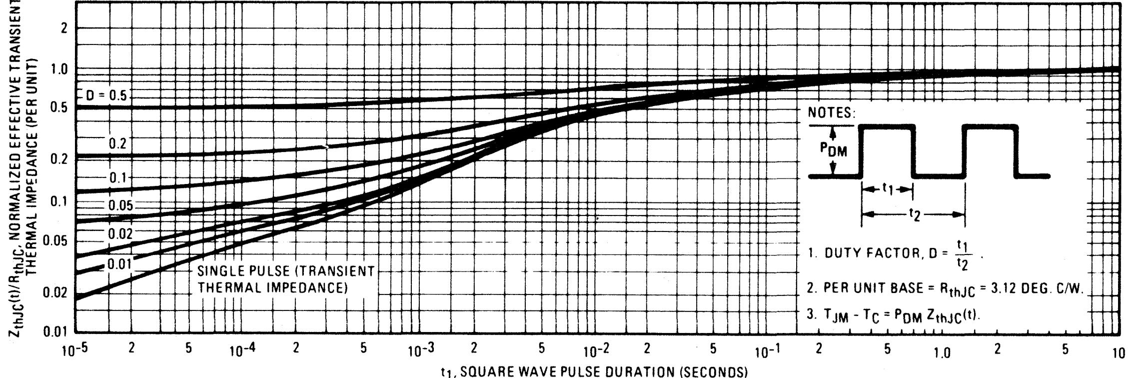


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

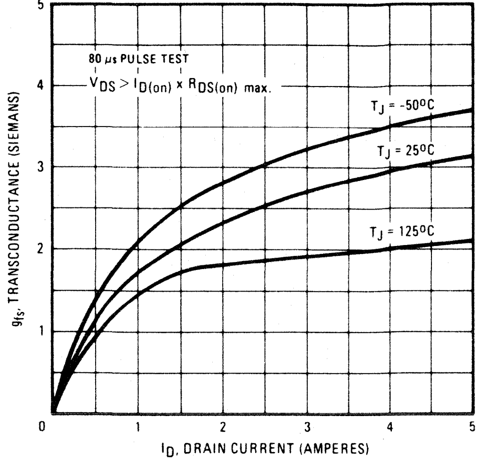


Fig. 6 — Typical Transconductance Vs. Drain Current

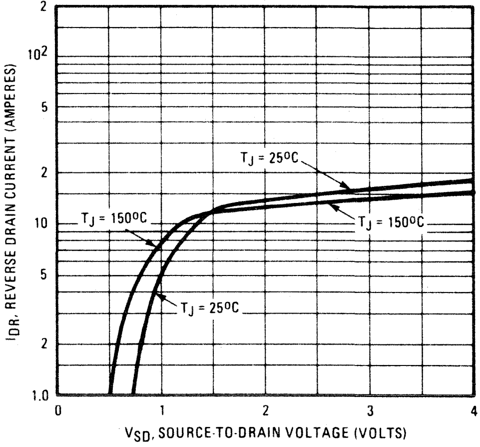


Fig. 7 — Typical Source-Drain Diode Forward Voltage

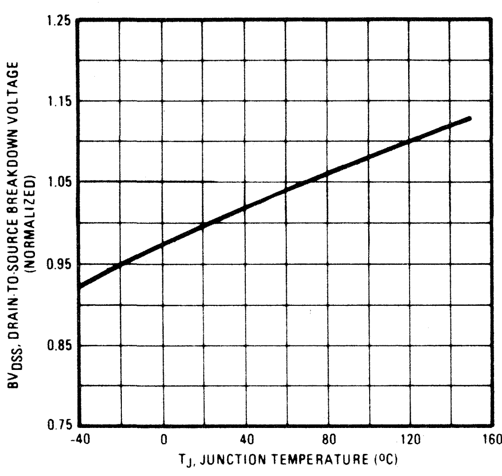


Fig. 8 — Breakdown Voltage Vs. Temperature

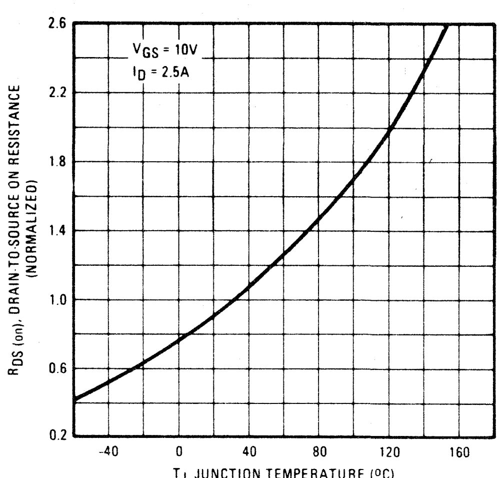


Fig. 9 — Normalized On-Resistance Vs. Temperature

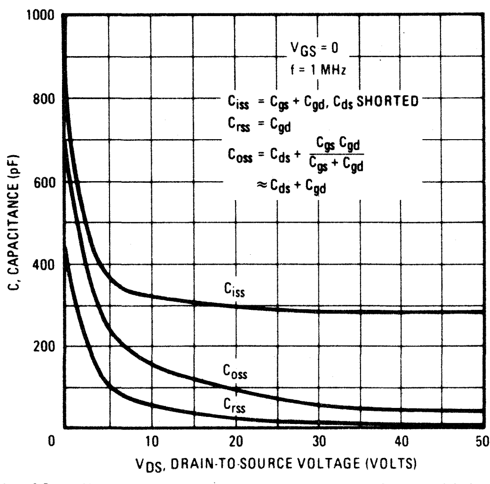


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

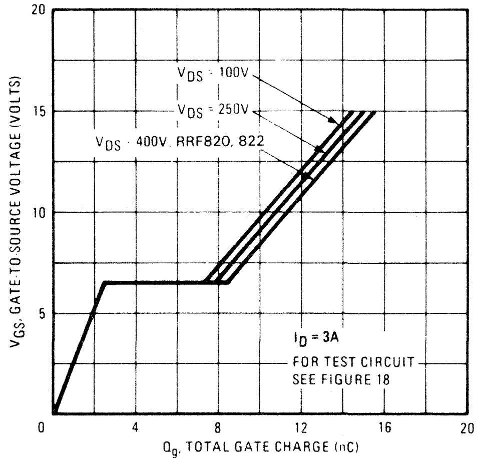


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

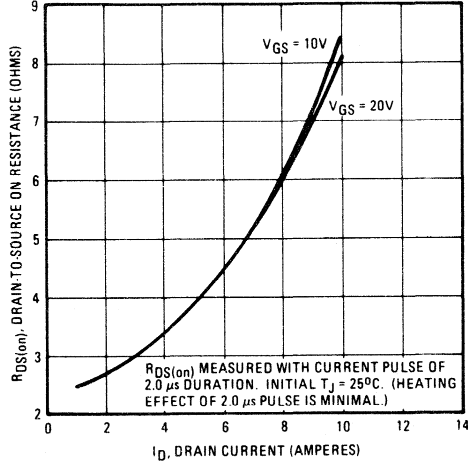


Fig. 12 – Typical On-Resistance Vs. Drain Current

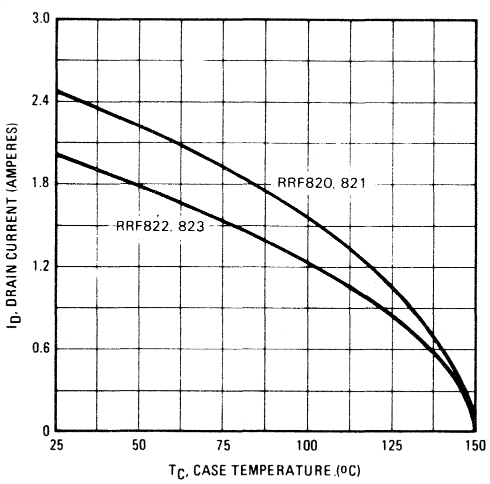


Fig. 13 – Maximum Drain Current Vs. Case Temperature

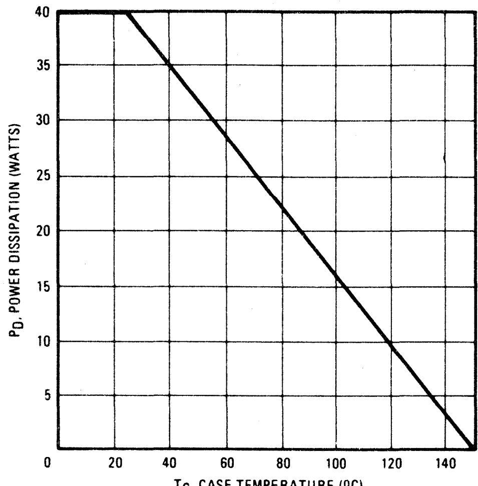


Fig. 14 – Power Vs. Temperature Derating Curve

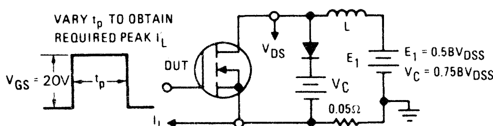


Fig. 15 – Clamped Inductive Test Circuit

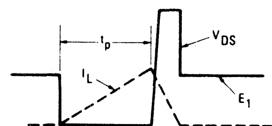


Fig. 16 – Clamped Inductive Waveforms

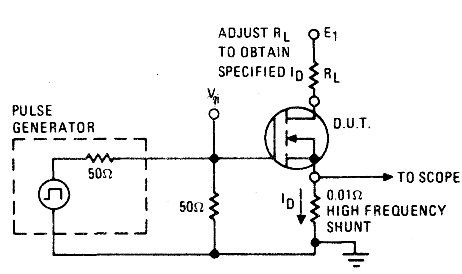


Fig. 17 – Switching Time Test Circuit

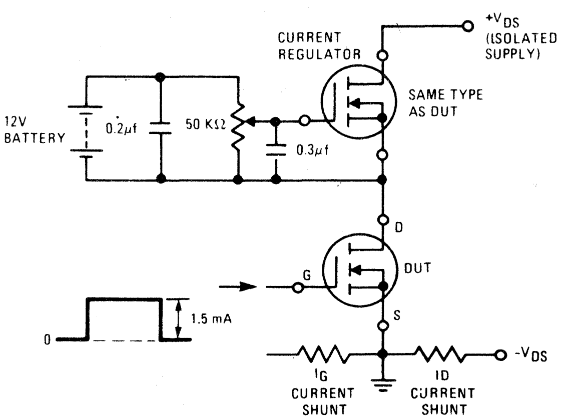


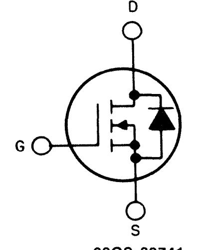
Fig. 18 – Gate Charge Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

The RRF830, RRF831, RRF832 and RRF833* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RRF-types are supplied in the JEDEC TO-220AB plastic package.

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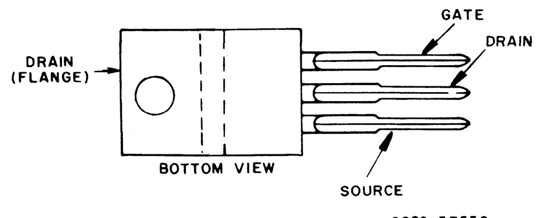
*These devices are equivalent to International Rectifier Power MOSFETs IRF830, IRF831, IRF832 and IRF833, and may be used as replacements therefore.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

Absolute Maximum Ratings

Parameter		RRF830	RRF831	RRF832	RRF833	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100µH	18	18	16	16	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

*** These types available 1st quarter 1985.**

RRF830, RRF831, RRF832, RRF833

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	RRF830 RRF832	500	–	–	V	V_{GS} = 0V
		RRF831 RRF833	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	RRF830 RRF831	4.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		RRF832 RRF833	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	RRF830 RRF831	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		RRF832 RRF833	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die. / Modified MOSFET symbol showing the internal device inductances.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	RRF830 RRF831	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		RRF832 RRF833	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	RRF830 RRF831	–	–	18	A	
		RRF832 RRF833	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	RRF830 RRF831	–	–	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		RRF832 RRF833	–	–	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

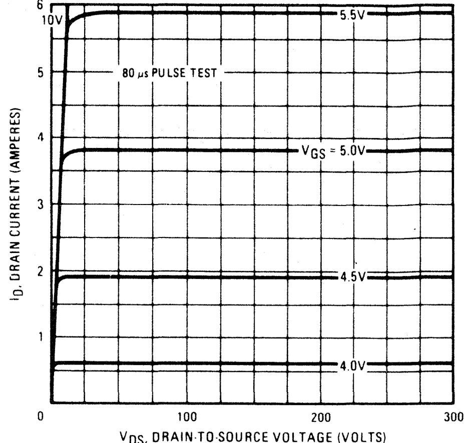


Fig. 1 — Typical Output Characteristics

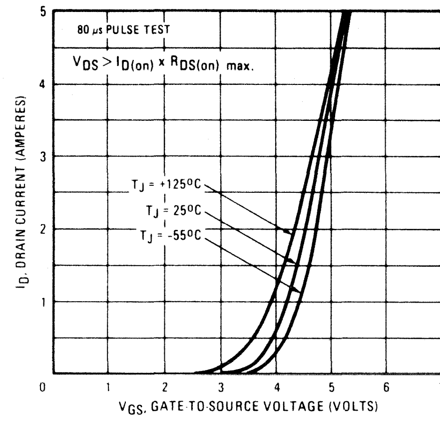


Fig. 2 — Typical Transfer Characteristics

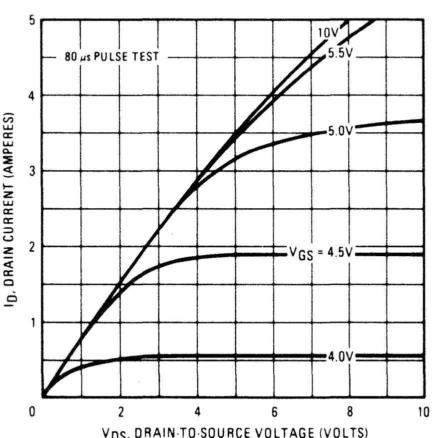


Fig. 3 — Typical Saturation Characteristics

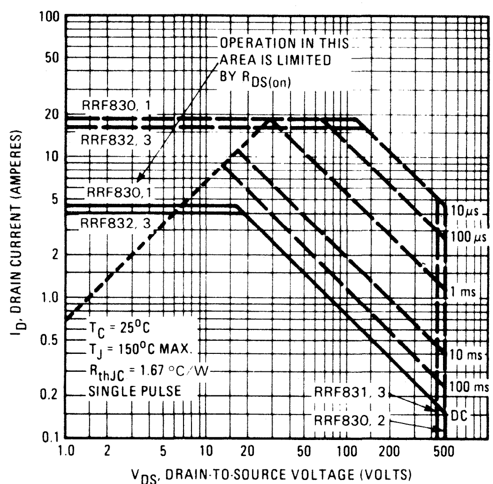


Fig. 4 — Maximum Safe Operating Area

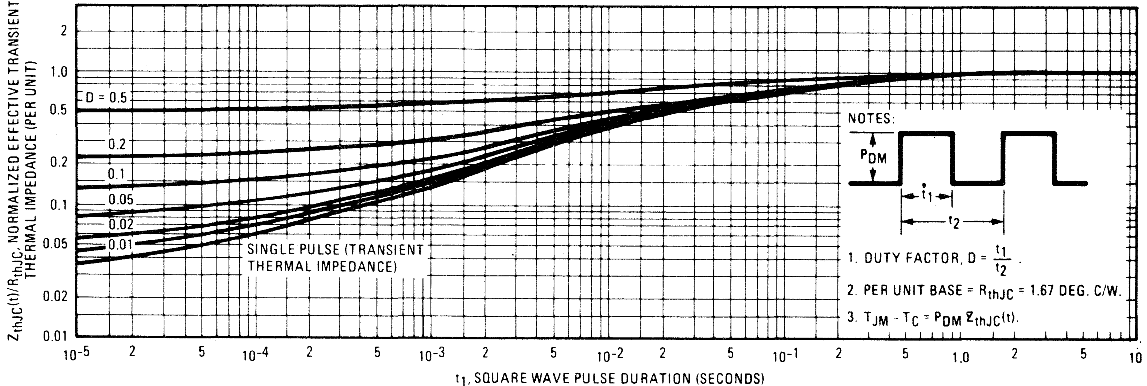


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

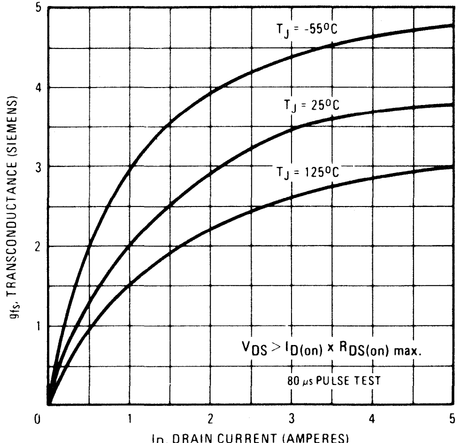


Fig. 6 — Typical Transconductance Vs. Drain Current

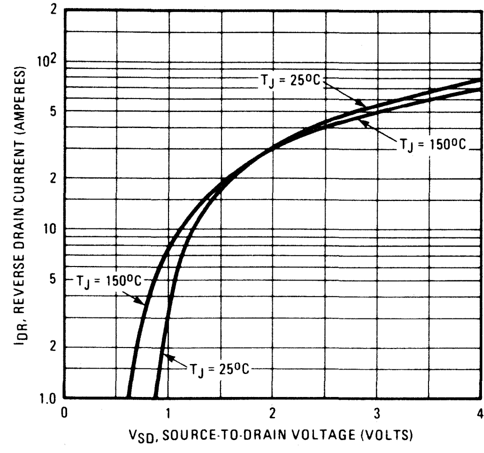


Fig. 7 — Typical Source-Drain Diode Forward Voltage

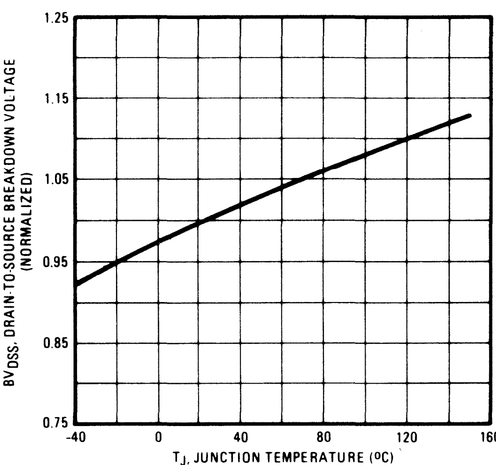


Fig. 8 — Breakdown Voltage Vs. Temperature

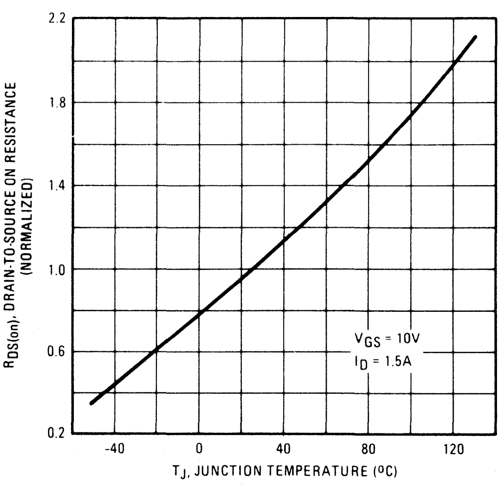


Fig. 9 — Normalized On-Resistance Vs. Temperature

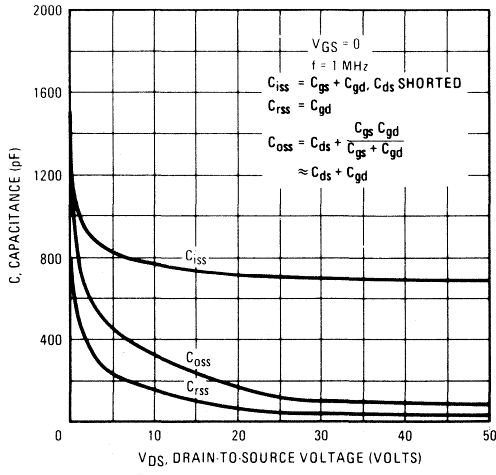


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

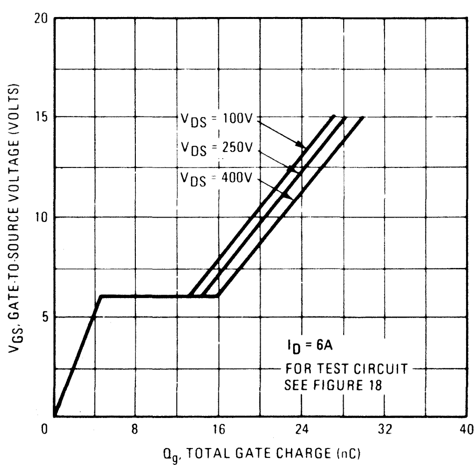


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

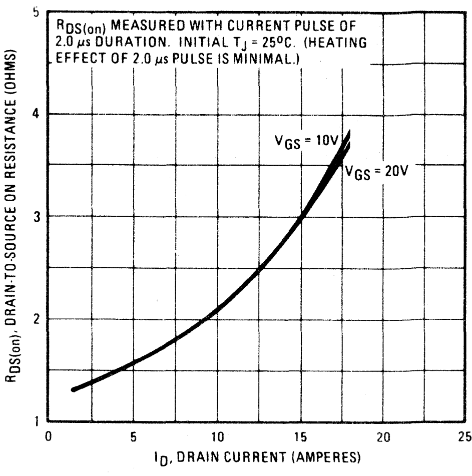


Fig. 12 — Typical On-Resistance Vs. Drain Current

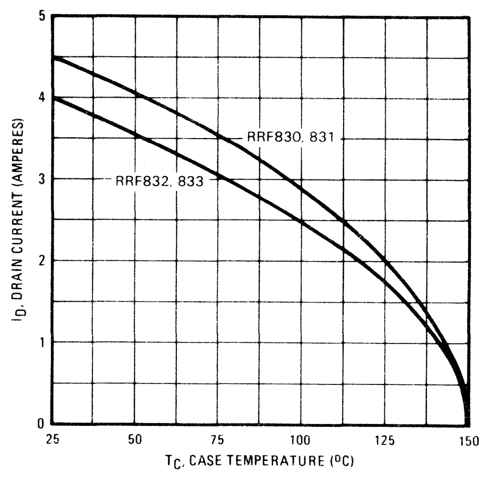


Fig. 13 — Maximum Drain Current Vs. Case Temperature

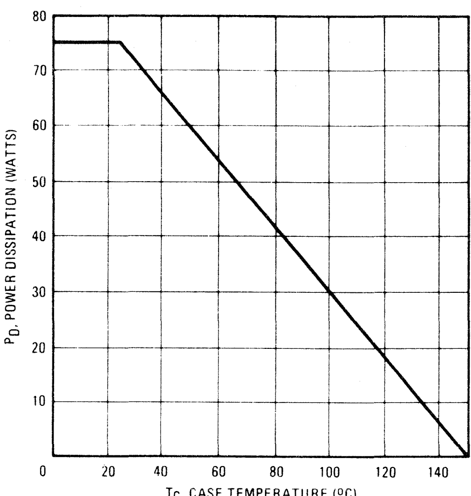


Fig. 14 — Power Vs. Temperature Derating Curve

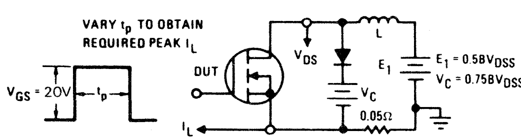


Fig. 15 — Clamped Inductive Test Circuit

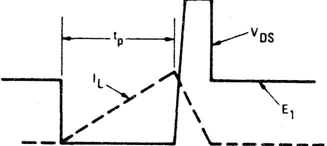


Fig. 16 — Clamped Inductive Waveforms

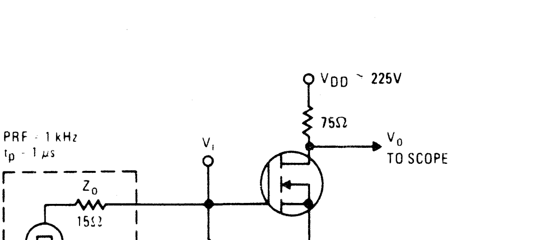


Fig. 17 — Switching Time Test Circuit

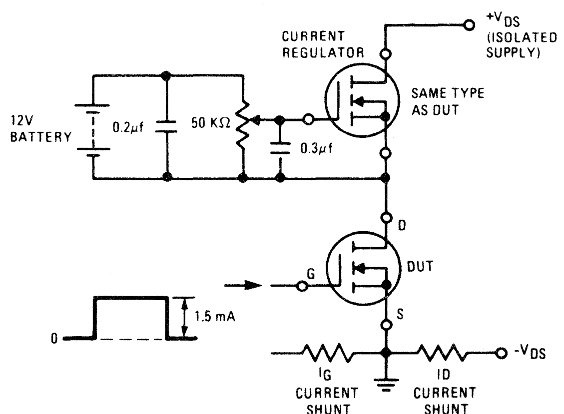


Fig. 18 — Gate Charge Test Circuit

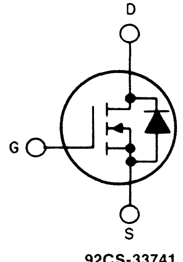
N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V - 100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

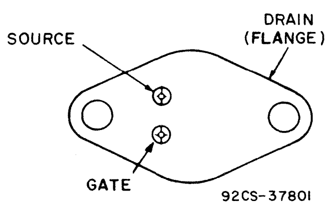


N-CHANNEL ENHANCEMENT MODE

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

	Parameter	2N6755	2N6756	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain Gate Voltage (R_{GS} 20 KΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0*	9.0*	A
I_{DM}	Pulsed Drain Current	25	30	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W °C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 25	30	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d\,(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 36V, I_D = 9A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	75*	ns	(See Figs. 13 and 14)
$t_{d\,(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	45*	ns	independent of operating temperature.)

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage (1)	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	µC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/µs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%

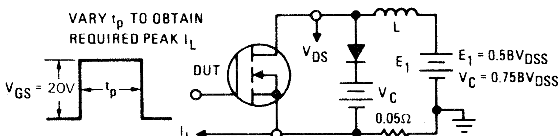


Fig. 1 — Clamped Inductive Test Circuit

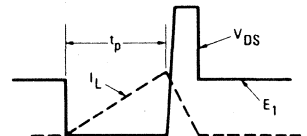


Fig. 2 — Clamped Inductive Waveforms

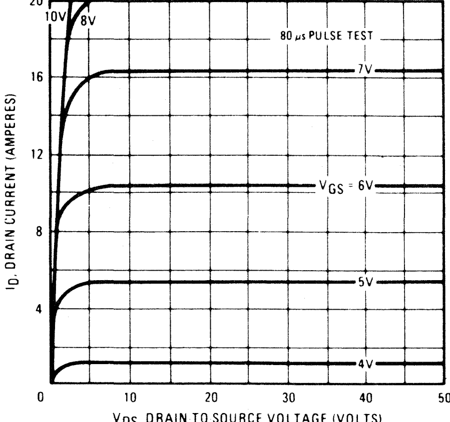


Fig. 3 — Typical Output Characteristics

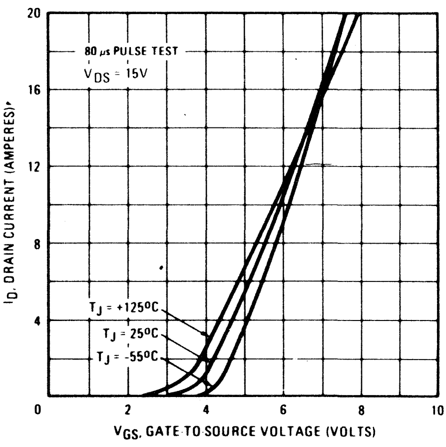


Fig. 4 — Typical Transfer Characteristics

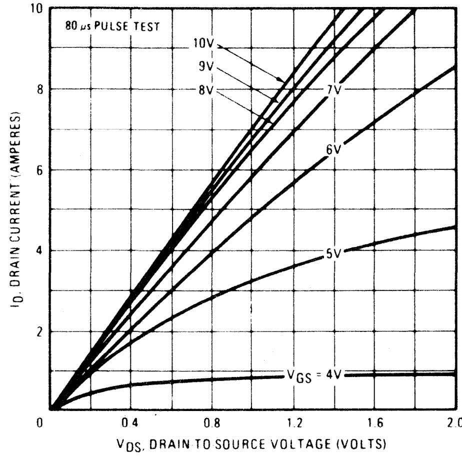


Fig. 5— Typical Saturation Characteristics (2N6755)

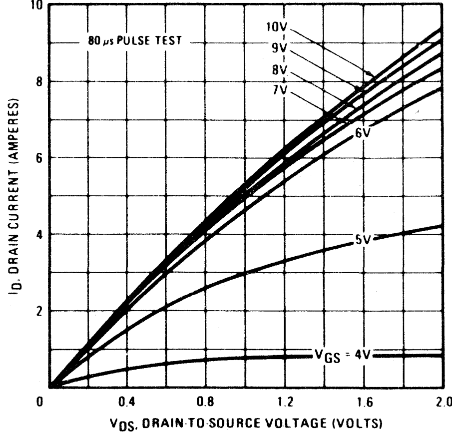


Fig. 6— Typical Saturation Characteristics (2N6756)

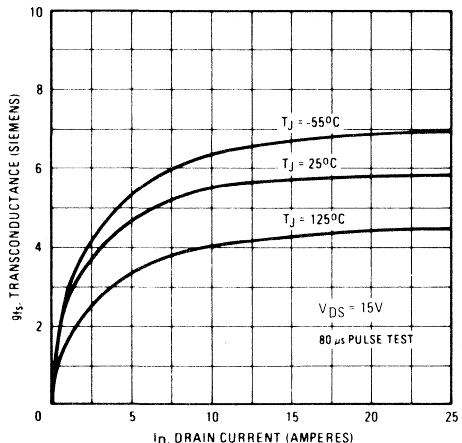


Fig. 7 — Typical Transconductance Vs. Drain Current

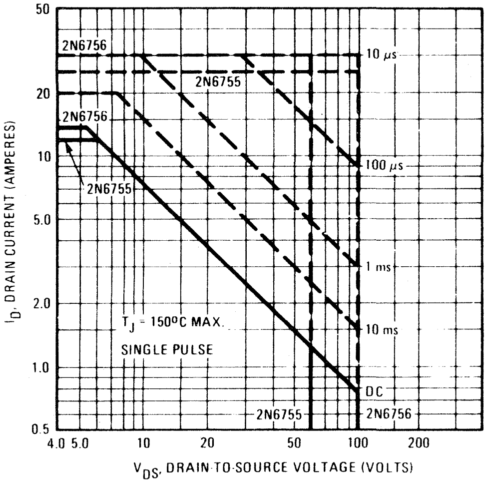


Fig. 8 — Maximum Safe Operating Area

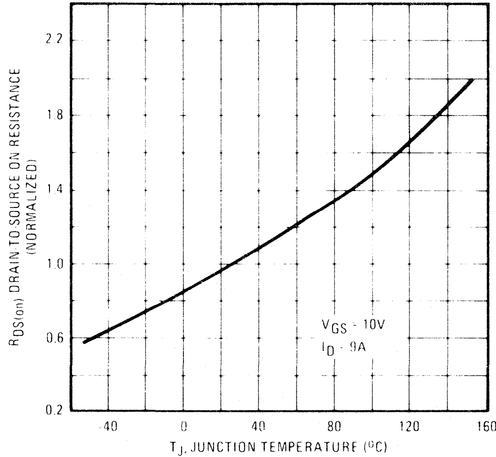


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

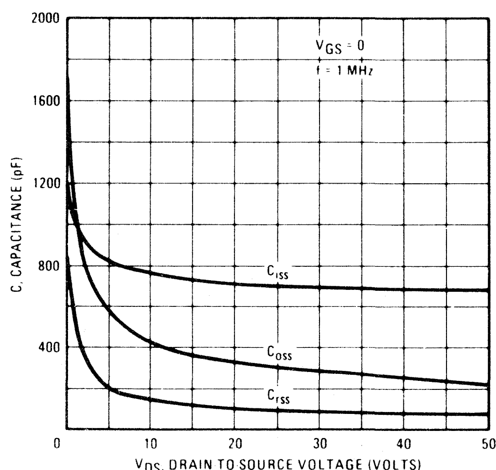


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

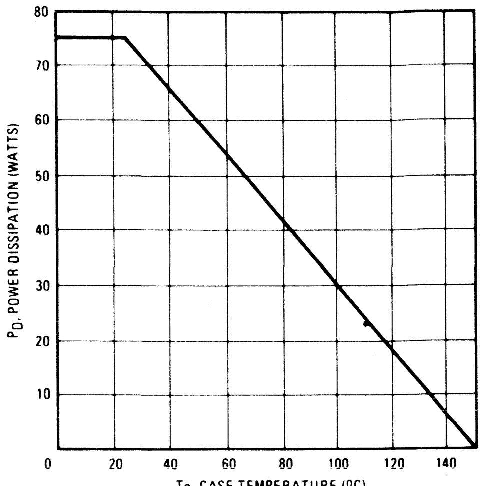


Fig. 11 – Power Vs. Temperature Derating Curve

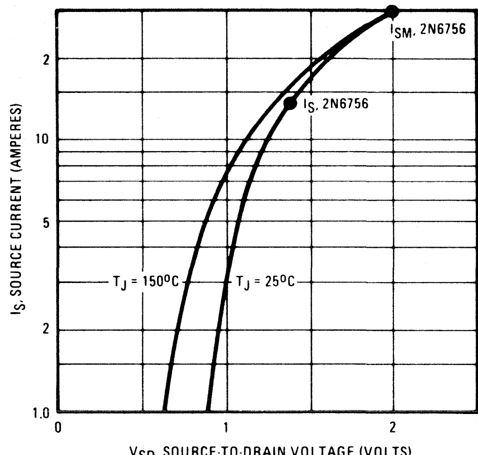


Fig. 12 – Typical Body-Drain Diode Forward Voltage

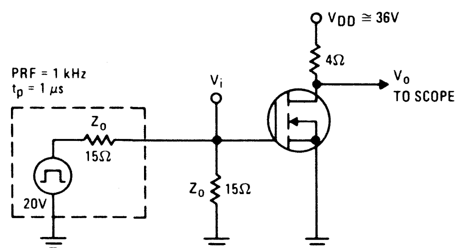


Fig. 13 – Switching Time Test Circuit

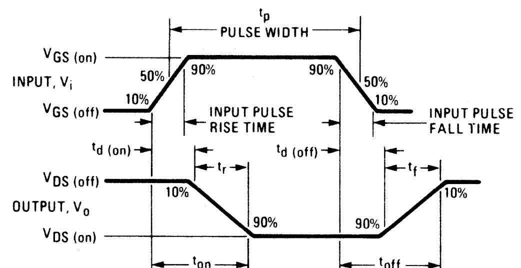


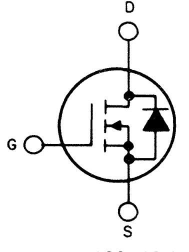
Fig. 14 – Switching Time Waveforms

N-Channel Enhancement-Mode Power Field-Effect Transistors

8A and 9A, 150V - 200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

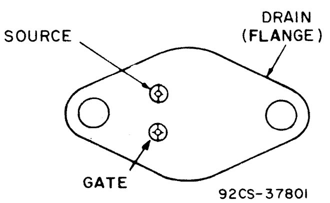


N-CHANNEL ENHANCEMENT MODE

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6757	2N6758	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I_{DM}	Pulsed Drain Current	12	15	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 12	15	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	$V_{GS} = 0$
		2N6758	200	–	–	V	$I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6757	–	–	4.8*	V	$V_{GS} = 10V$, $I_D = 8A$
		2N6758	–	–	3.6*	V	$V_{GS} = 10V$, $I_D = 9A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6757	–	0.4	0.6*	Ω	$V_{GS} = 10V$, $I_D = 5A$
		2N6758	–	0.25	0.4*	Ω	$V_{GS} = 10V$, $I_D = 6A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6757	–	–	1.13*	Ω	$V_{GS} = 10V$, $I_D = 5A$, $T_C = 125^oC$
		2N6758	–	–	0.75*	Ω	$V_{GS} = 10V$, $I_D = 6A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	3.0*	5.0	9.0*	S (℧)	$V_{DS} = 15V$, $I_D = 6A$
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 90V$, $I_D = 6A$, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	40*	ns	independent of operating temperature.)

Thermal Resistance

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

Symbol	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage (1)	2N6757	0.75*	–	1.50*	V	$T_C = 25^oC$, $I_S = 8A$, $V_{GS} = 0$
		2N6758	0.80*	–	1.60*	V	$T_C = 25^oC$, $I_S = 9A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

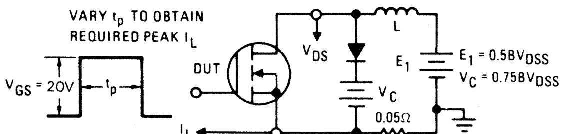


Fig. 1 — Clamped Inductive Test Circuit

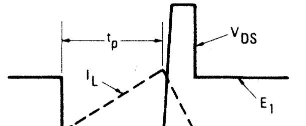


Fig. 2 — Clamped Inductive Waveforms

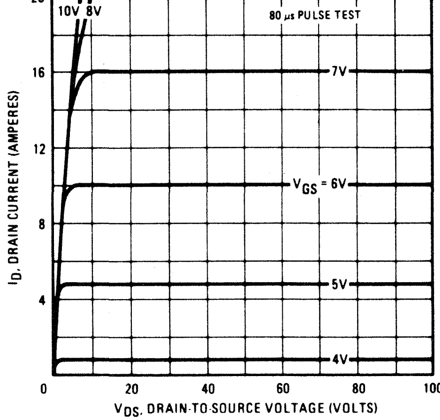


Fig. 3 — Typical Output Characteristics

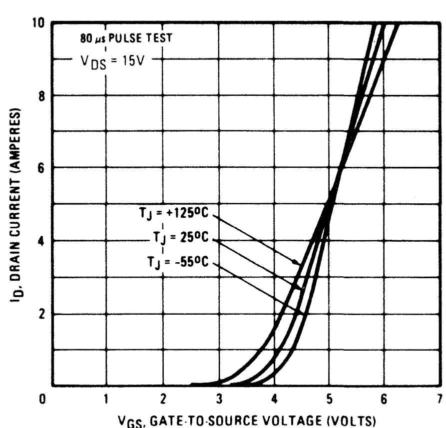


Fig. 4 — Typical Transfer Characteristics

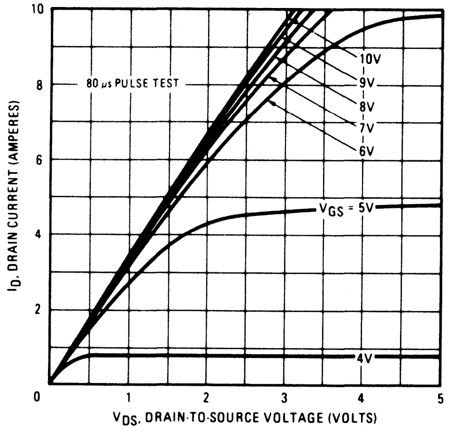


Fig. 5— Typical Saturation Characteristics (2N6757)

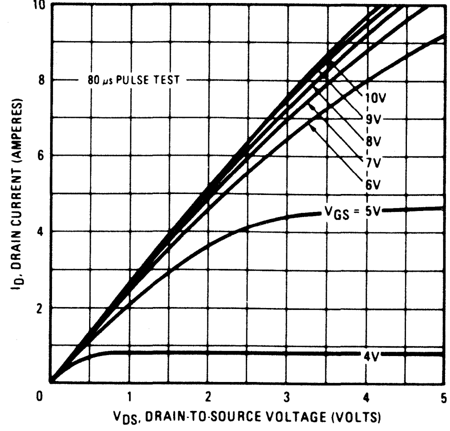


Fig. 6— Typical Saturation Characteristics (2N6758)

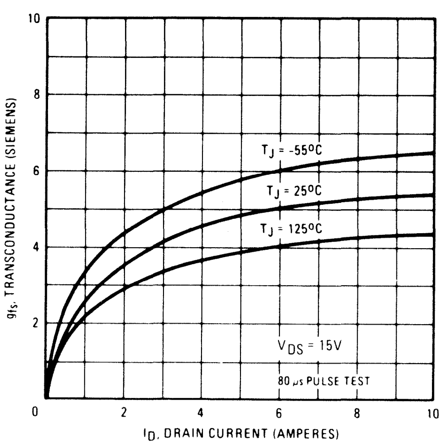


Fig. 7 — Typical Transconductance Vs. Drain Current

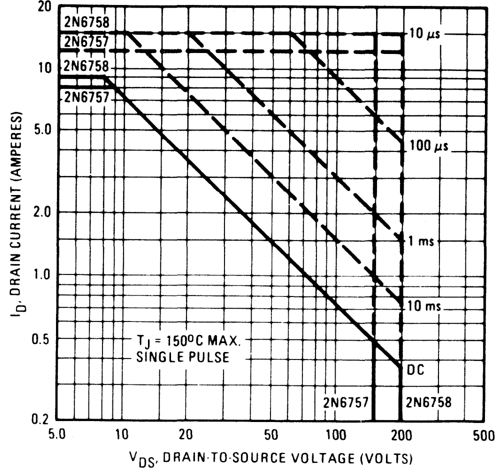


Fig. 8 — Maximum Safe Operating Area

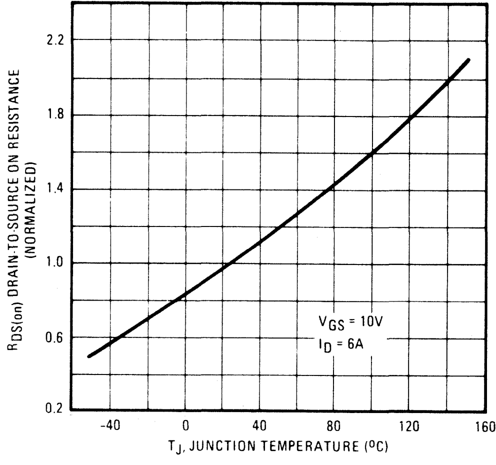


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

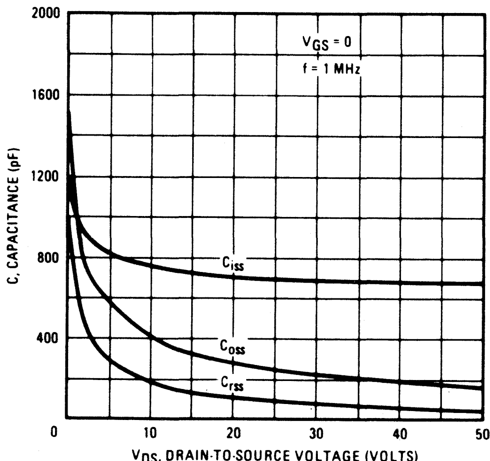


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

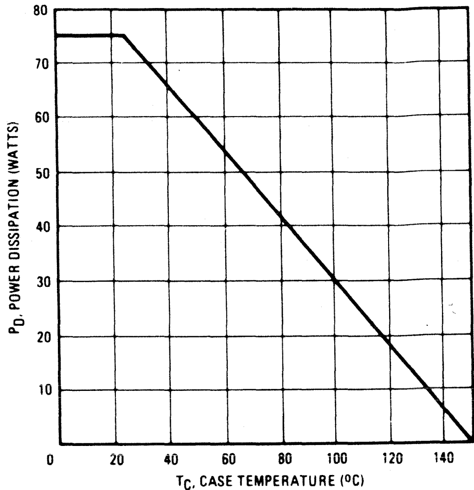


Fig. 11 — Power Vs. Temperature Derating Curve

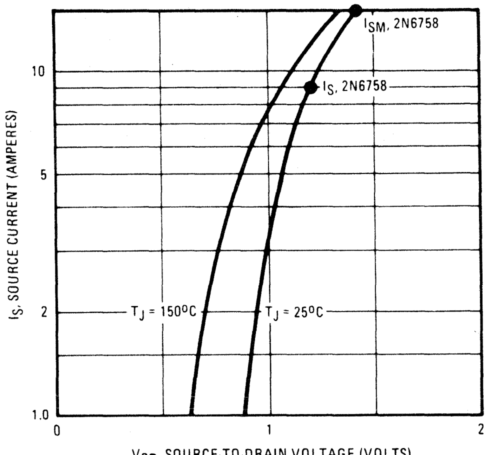


Fig. 12 — Typical Body-Drain Diode Forward Voltage

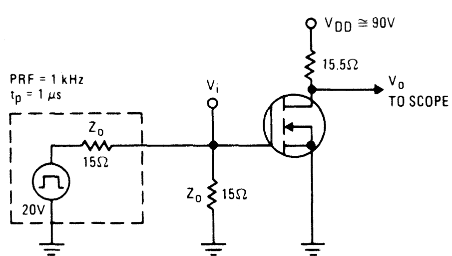


Fig. 13 — Switching Time Test Circuit

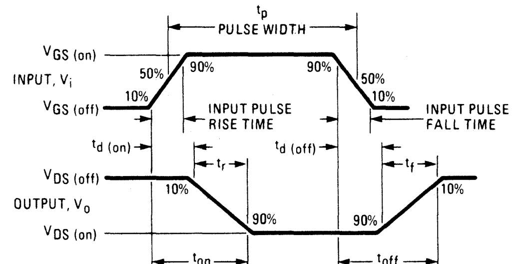


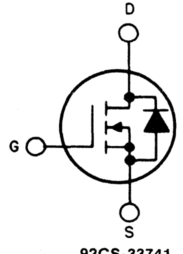
Fig. 14 — Switching Time Waveforms

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V - 400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

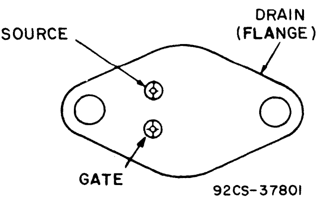


N-CHANNEL ENHANCEMENT MODE

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6759	2N6760	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5*	5.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0*	3.5*	A
I_{DM}	Pulsed Drain Current	7.0	8.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 7.0	8.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	$V_{GS} = 0$
		2N6760	400	–	–	V	$I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6759	–	–	7.0*	V	$V_{GS} = 10V$, $I_D = 4.5A$
		2N6760	–	–	6.7*	V	$V_{GS} = 10V$, $I_D = 5.5A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	1.0	1.5*	Ω	$V_{GS} = 10V$, $I_D = 3A$
		2N6760	–	0.8	1.0*	Ω	$V_{GS} = 10V$, $I_D = 3.5A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	–	3.3*	Ω	$V_{GS} = 10V$, $I_D = 3A$, $T_C = 125^oC$
		2N6760	–	–	2.2*	Ω	$V_{GS} = 10V$, $I_D = 3.5A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	3.0*	4.5	9.0*	S (℧)	$V_{DS} = 15V$, $I_D = 3.5A$
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 175V$, $I_D = 3.5A$, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage ①	2N6759	0.70*	–	1.4*	V	$T_C = 25^oC$, $I_S = 4.5A$, $V_{GS} = 0$
		2N6760	0.75*	–	1.5*	V	$T_C = 25^oC$, $I_S = 5.5A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	µC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/µs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%

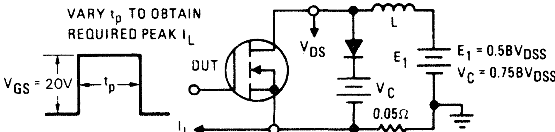


Fig. 1 — Clamped Inductive Test Circuit

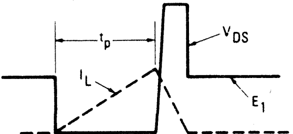


Fig. 2 — Clamped Inductive Waveforms

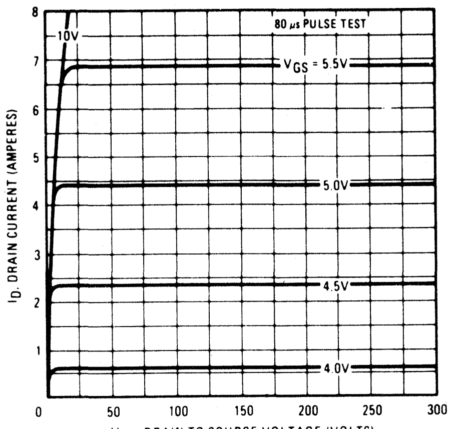


Fig. 3 — Typical Output Characteristics

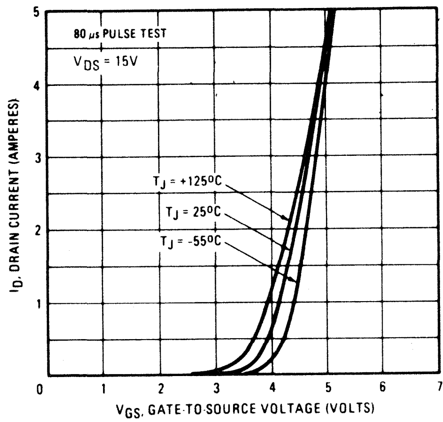


Fig. 4 — Typical Transfer Characteristics

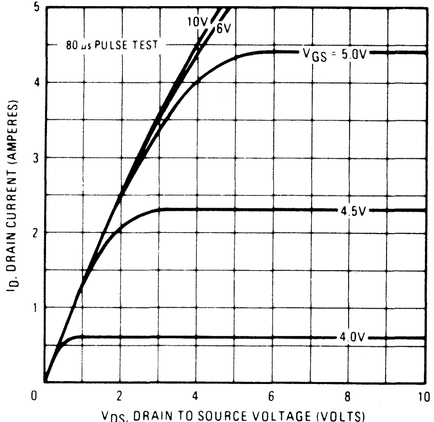


Fig. 5— Typical Saturation Characteristics (2N6759)

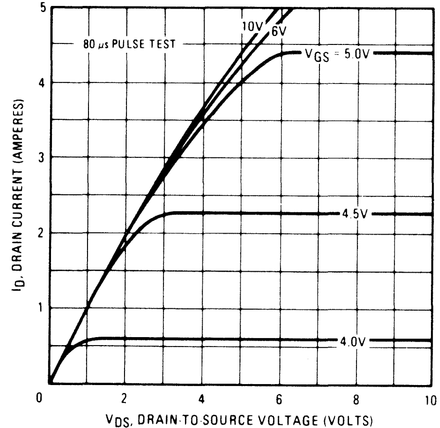


Fig. 6— Typical Saturation Characteristics (2N6760)

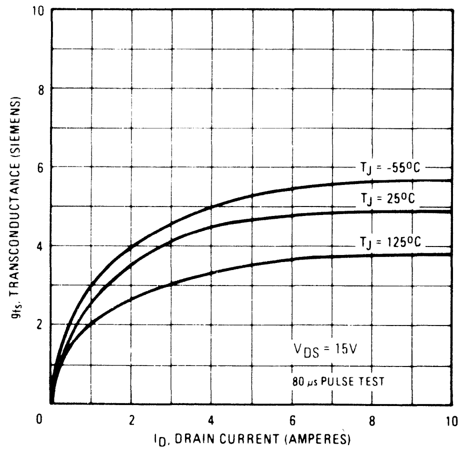


Fig. 7 — Typical Transconductance Vs. Drain Current

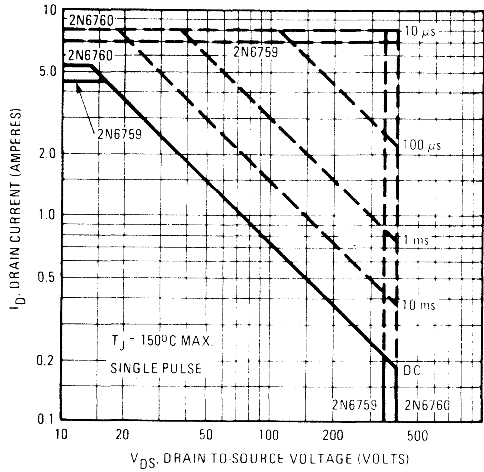


Fig. 8 — Maximum Safe Operating Area

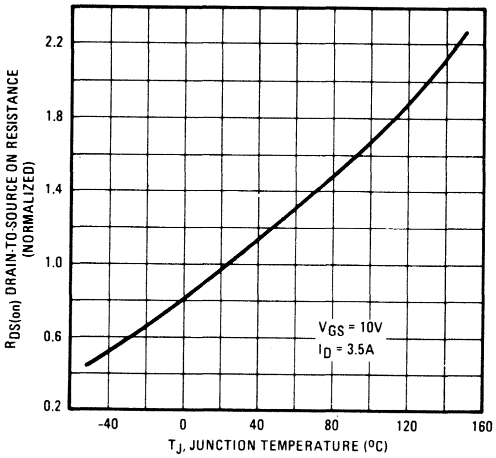


Fig.9—Normalized Typical On-Resistance Vs. Temperature

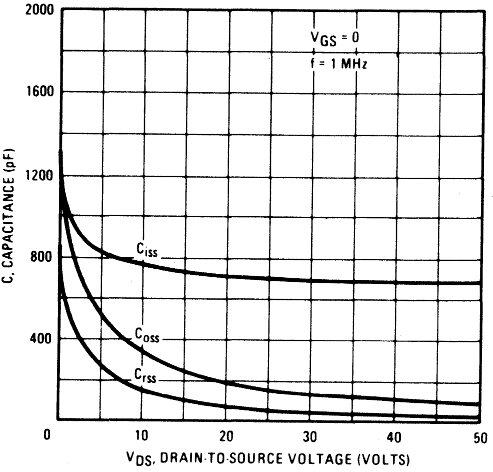


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

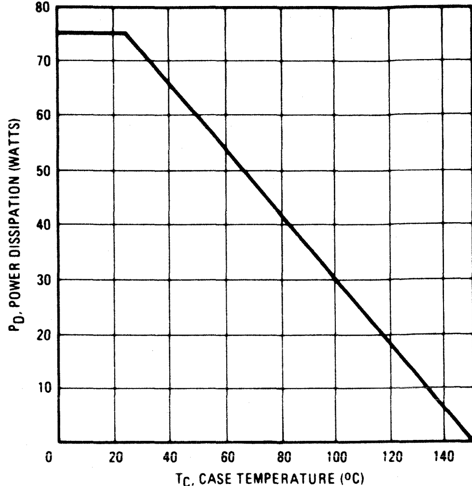


Fig. 11 — Power Vs. Temperature Derating Curve

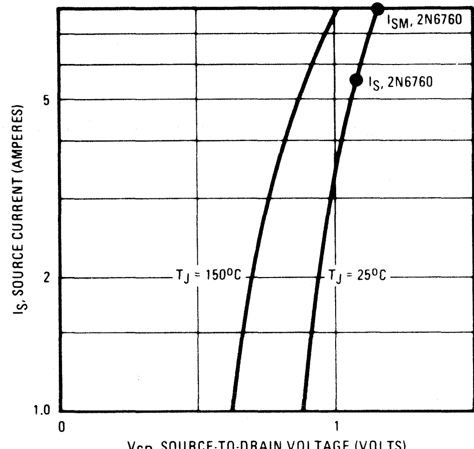


Fig. 12 — Typical Body-Drain Diode Forward Voltage

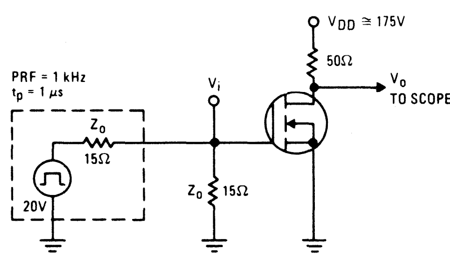


Fig. 13 — Switching Time Test Circuit

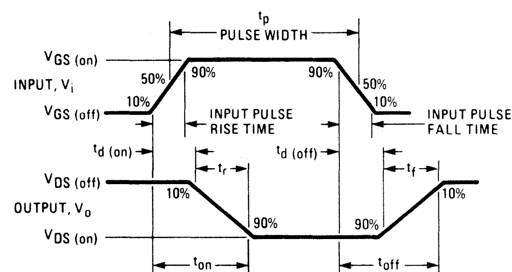


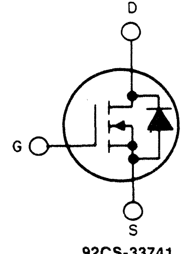
Fig. 14 — Switching Time Waveforms

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 4.5A, 450V - 500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

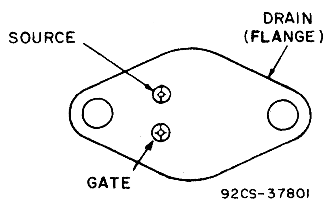


N-CHANNEL ENHANCEMENT MODE

The 2N6761 and 2N6762 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6761	2N6762	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0*	4.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5*	3.0*	A
I_{DM}	Pulsed Drain Current	6.0	7.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 6.0	7.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

*** These types available 1st quarter 1985.**

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	$V_{GS} = 0$
		2N6762	500	–	–	V	$I_D = 4.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	$V_{DS} = 0.8 \times$ Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 25^oC$ to 125^oC
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6761	–	–	8.0*	V	$V_{GS} = 10V$, $I_D = 4A$
		2N6762	–	–	7.7*	V	$V_{GS} = 10V$, $I_D = 4.5A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6761	–	1.5	2.0*	Ω	$V_{GS} = 10V$, $I_D = 2.5A$
		2N6762	–	1.3	1.5*	Ω	$V_{GS} = 10V$, $I_D = 3.0A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6761	–	–	4.4*	Ω	$V_{GS} = 10V$, $I_D = 2.5A$, $T_C = 125^oC$
		2N6762	–	–	3.3*	Ω	$V_{GS} = 10V$, $I_D = 3.0A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	2.5*	3.5	7.5*	S (℧)	$V_{DS} = 16V$, $I_D = 3A$
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 225V$, $I_D = 3A$, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	30*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	30*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage (1)	2N6761	0.65*	–	1.3*	V	$T_C = 25^oC$, $I_S = 4A$, $V_{GS} = 0$
		2N6762	0.7*	–	1.4*	V	$T_C = 25^oC$, $I_S = 4.5A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

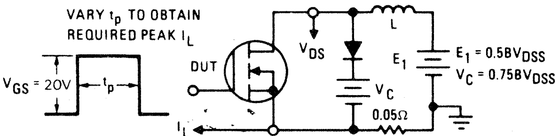


Fig. 1 — Clamped Inductive Test Circuit

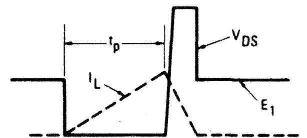


Fig. 2 — Clamped Inductive Waveforms

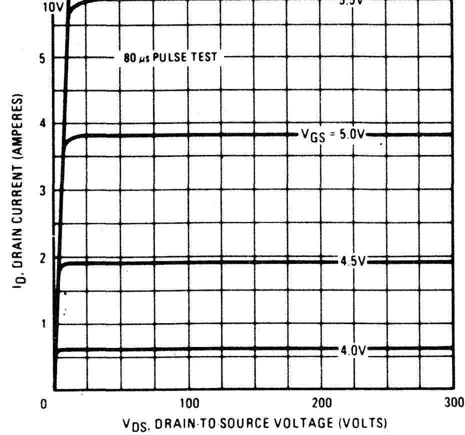


Fig. 3 — Typical Output Characteristics

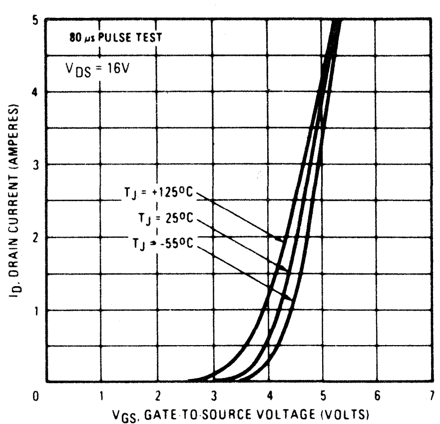


Fig. 4 — Typical Transfer Characteristics

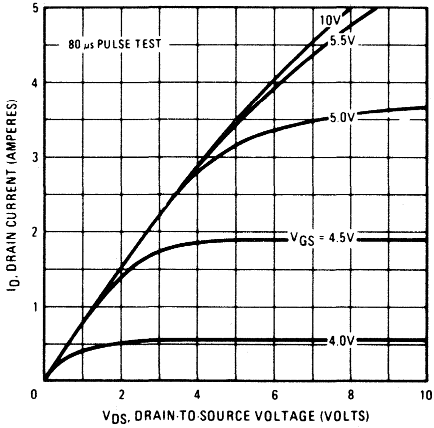


Fig. 5— Typical Saturation Characteristics (2N6761)

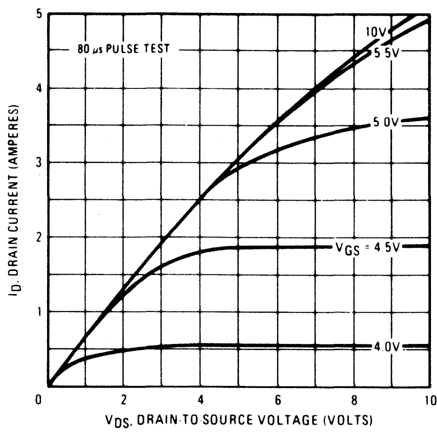


Fig. 6— Typical Saturation Characteristics (2N6762)

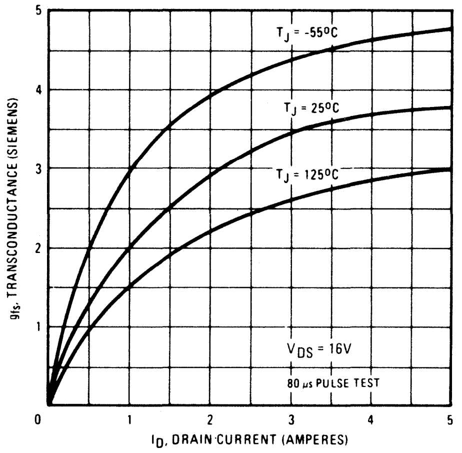


Fig. 7 — Typical Transconductance Vs. Drain Current

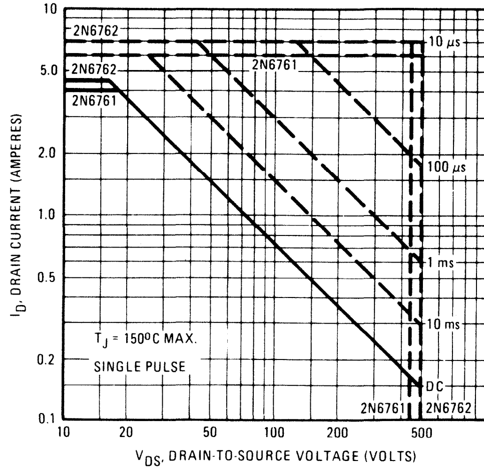


Fig. 8 — Maximum Safe Operating Area

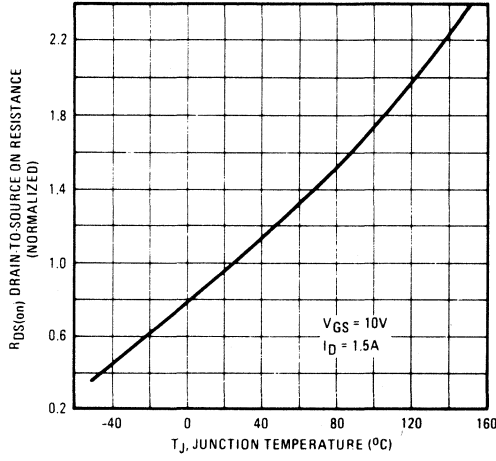


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

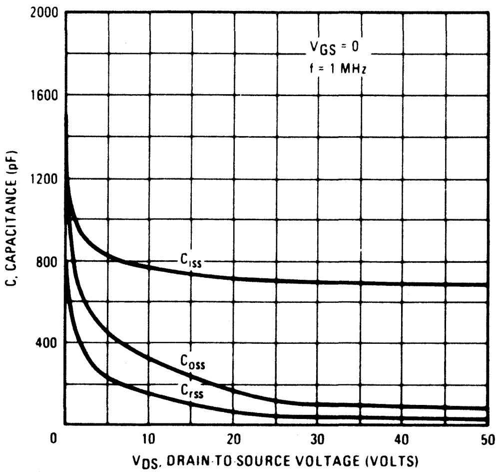


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

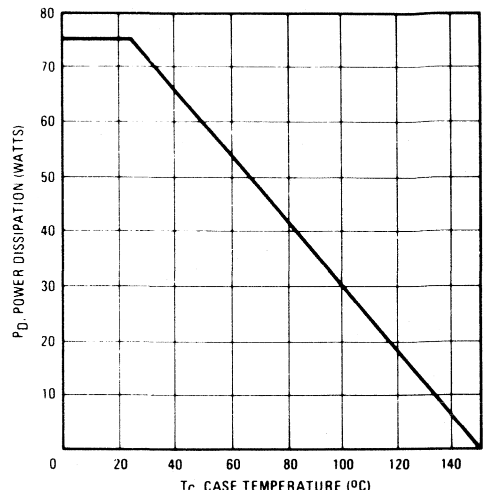


Fig. 11 — Power Vs. Temperature Derating Curve

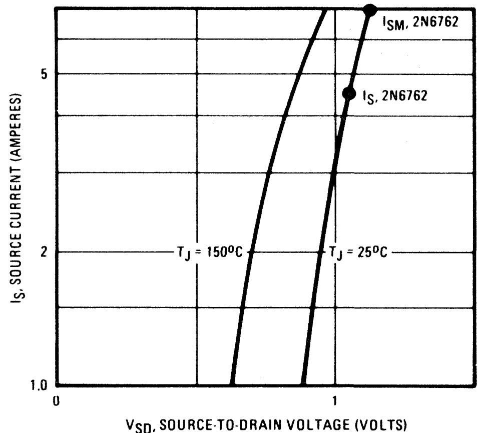


Fig. 12 — Typical Body-Drain Diode Forward Voltage

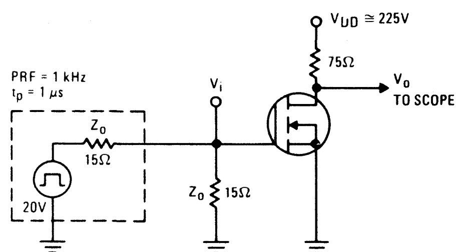


Fig. 13 — Switching Time Test Circuit

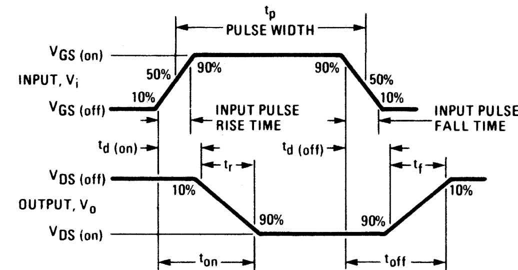


Fig. 14 — Switching Time Waveforms

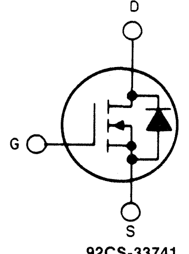
N-Channel Enhancement-Mode Power Field-Effect Transistors

38A, 100V

$r_{DS}(on) = 0.055\ \Omega$

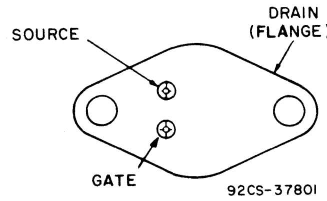
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-204AE

The 2N6764 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6764 is supplied in the JEDEC TO-204AE steel package.

Absolute Maximum Ratings

Parameter		2N6764	Units
V_{DS}	Drain – Source Voltage	100*	V
V_{DGR}	Drain Gate Voltage (R_{GS} 20 KΩ)	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	38*	A
I_D @ T_C = 100°C	Continuous Drain Current	24*	A
I_{DM}	Pulsed Drain Current	70	A
V_{GS}	Gate – Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)	W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)	W
	Linear Derating Factor	1.2* (See Fig. 11)	W °C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60 | 70	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6764	100	–	–	V	$V_{GS} = 0$ $I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6764	–		2.09*	V	$V_{GS} = 10V$ $I_D = 31A$ $V_{GS} = 10V$, $I_D = 38A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6764	–	0.045	0.055*	Ω	$V_{GS} = 10V$, $I_D = 20A$ $V_{GS} = 10V$, $I_D = 24A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6764	–	–	0.094*	Ω	$V_{GS} = 10V$, $I_D = 20A$, $T_C = 125^oC$ $V_{GS} = 10V$, $I_D = 24A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	$V_{DS} = 15V$, $I_D = 24A$
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 24V$, $I_D = 24A$, $Z_o = 4.7\Omega$
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	2N6764	–	–	38*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (D, G, S)
I_{SM}	Pulsed Source Current (Body Diode)	2N6764	–	–	70	A	
V_{SD}	Diode Forward Voltage ①	2N6764	0.95*	–	1.9*	V	$T_C = 25^oC$, $I_S = 31A$, $V_{GS} = 0$
						V	$T_C = 25^oC$, $I_S = 38A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

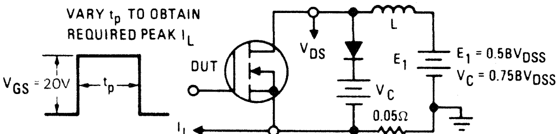


Fig. 1 — Clamped Inductive Test Circuit

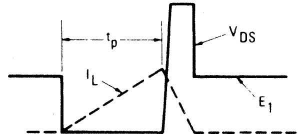


Fig. 2 — Clamped Inductive Waveforms

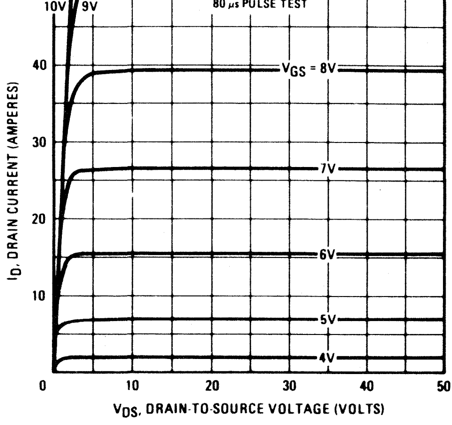


Fig. 3 — Typical Output Characteristics

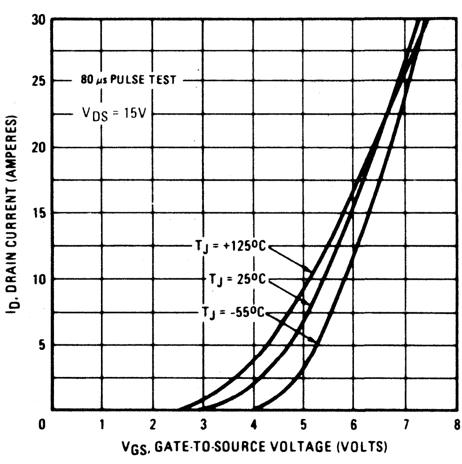


Fig. 4 — Typical Transfer Characteristics

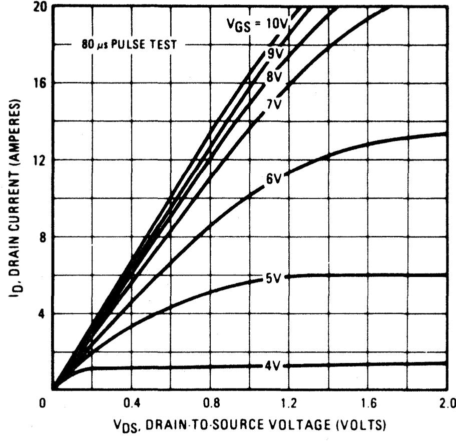


Fig. 5– Typical Saturation Characteristics (2N6764)

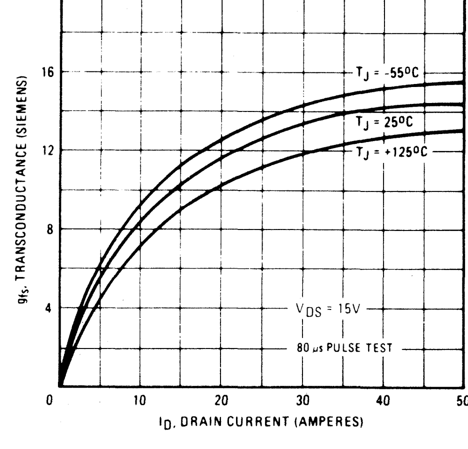


Fig. 6– Typical Transconductance Vs. Drain Current

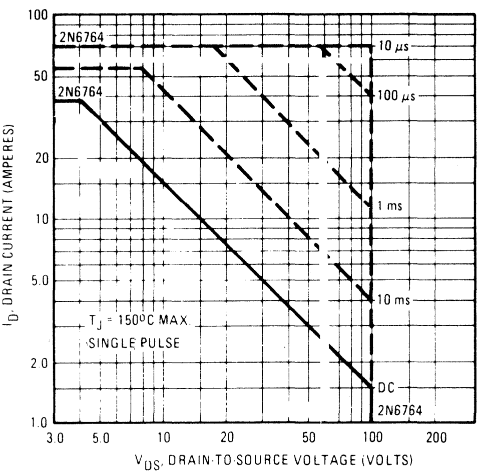


Fig. 7 – Maximum Safe Operating Area

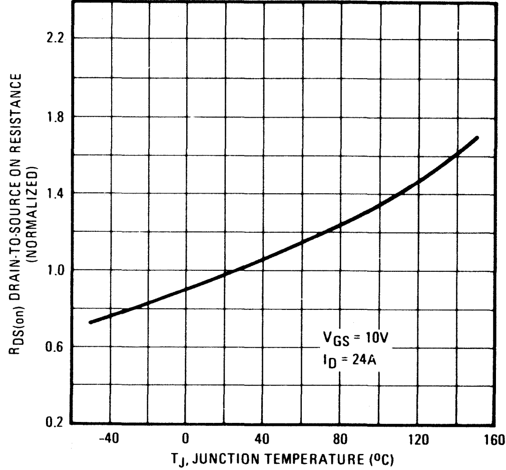


Fig. 8 – Normalized Typical On-Resistance Vs. Temperature

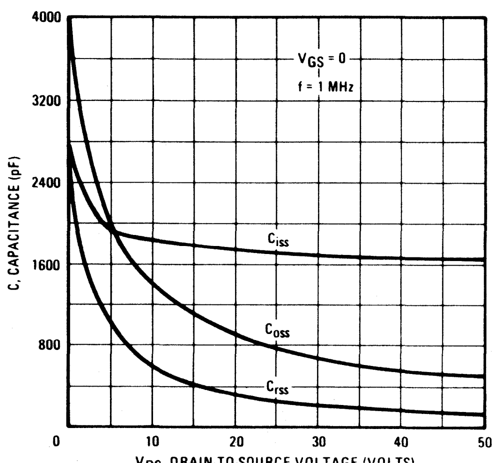


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

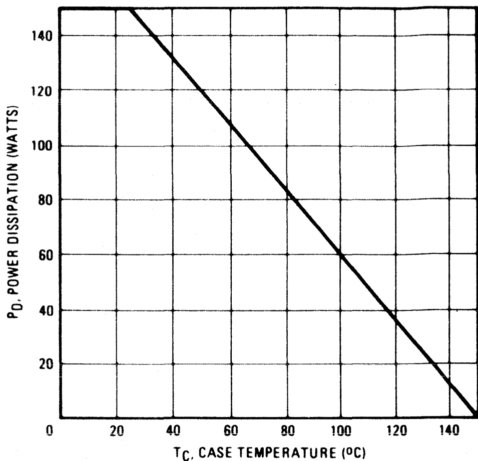


Fig. 10 – Power Vs. Temperature Derating Curve

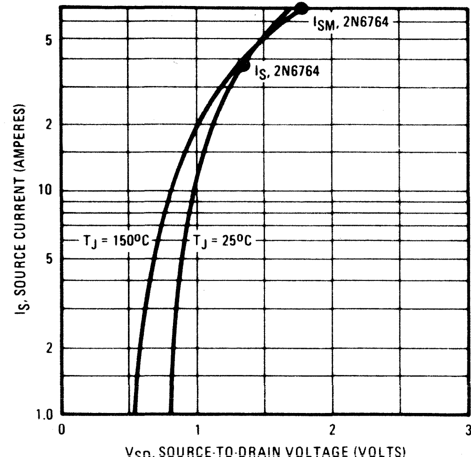


Fig. 11 – Typical Body-Drain Diode Forward Voltage

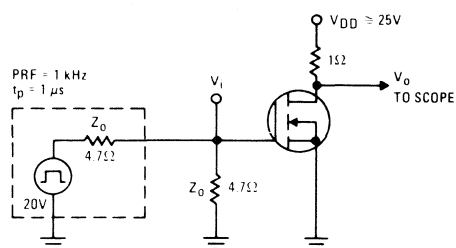


Fig. 12 – Switching Time Test Circuit

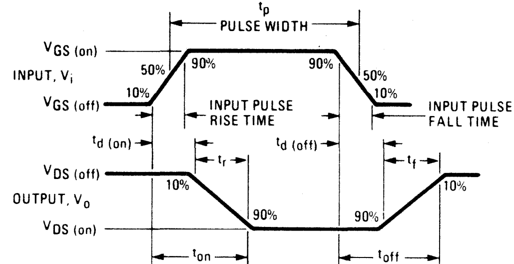


Fig. 13 – Switching Time Waveforms

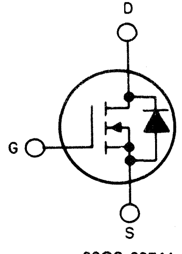
N-Channel Enhancement-Mode Power Field-Effect Transistors

30A, 200V

$r_{DS}(on) = 0.085\ \Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

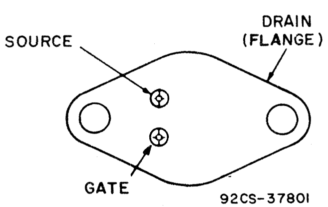


N-CHANNEL ENHANCEMENT MODE

The 2N6766 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6766 is supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

Absolute Maximum Ratings

	Parameter	2N6766	Units
V_{DS}	Drain – Source Voltage	200*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	30*	A
I_D @ T_C = 100°C	Continuous Drain Current	19*	A
I_{DM}	Pulsed Drain Current	60	A
V_{GS}	Gate – Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)	W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)	W
	Linear Derating Factor	1.2* (See Fig. 11)	W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH 50 | 60	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6766	200	–	–	V	$V_{GS} = 0$ $I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6766	–	–	2.7*	V	$V_{GS} = 10V$, $I_D = 25A$ $V_{GS} = 10V$, $I_D = 30A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6766	–	0.07	0.085*	Ω	$V_{GS} = 10V$, $I_D = 16A$ $V_{GS} = 10V$, $I_D = 19A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6766	–	–	0.153*	Ω	$V_{GS} = 10V$, $I_D = 16A$, $T_C = 125^oC$ $V_{GS} = 10V$, $I_D = 19A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	9.0*	15.5	27*	S (℧)	$V_{DS} = 15V$, $I_D = 19A$
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d\,(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 95V$, $I_D = 19A$, $Z_o = 4.7Ω$
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\,(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	2N6766	–	–	30*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (G, D, S)
I_{SM}	Pulsed Source Current (Body Diode)	2N6766	–	–	60	A	
V_{SD}	Diode Forward Voltage (1)	2N6766	0.9*	–	1.8*	V	$T_C = 25^oC$, $I_S = 25A$, $V_{GS} = 0$ $T_C = 25^oC$, $I_S = 30A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

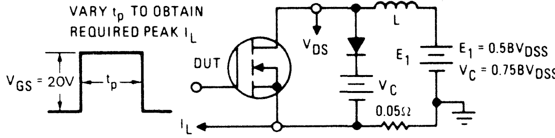


Fig. 1 — Clamped Inductive Test Circuit

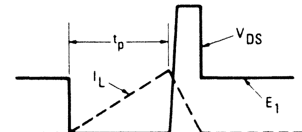


Fig. 2 — Clamped Inductive Waveforms

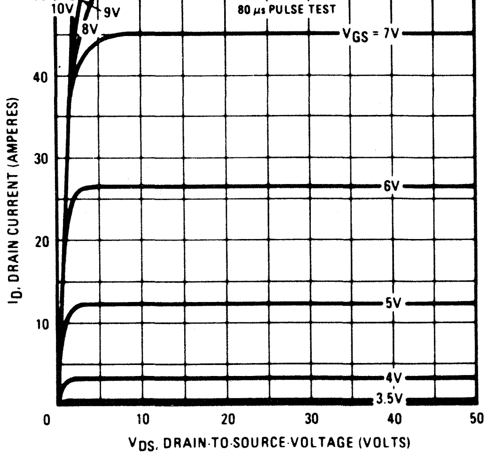


Fig. 3 — Typical Output Characteristics

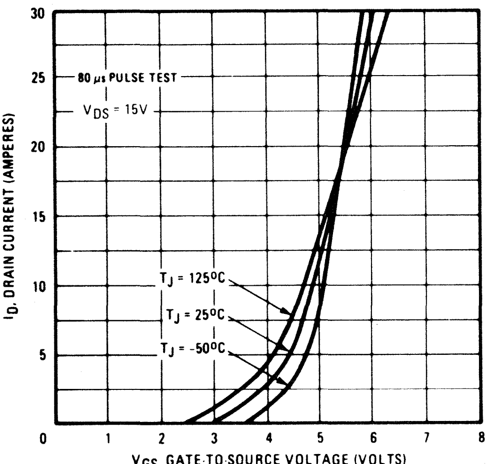


Fig. 4 — Typical Transfer Characteristics

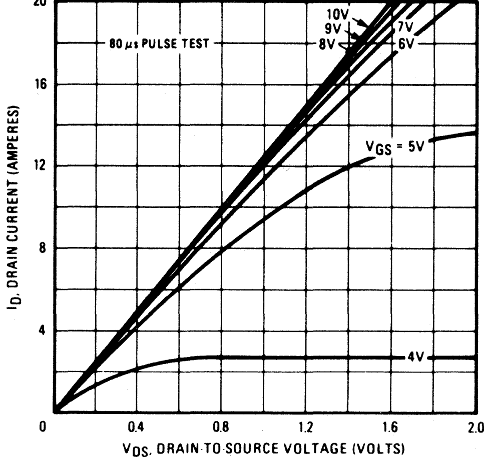


Fig. 5— Typical Saturation Characteristics (2N6765)

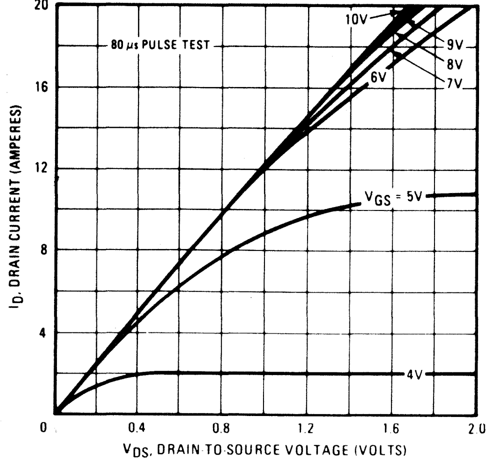


Fig. 6— Typical Saturation Characteristics (2N6766)

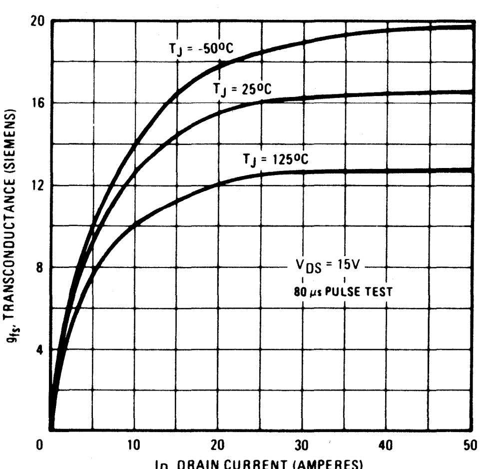


Fig. 7 — Typical Transconductance Vs. Drain Current

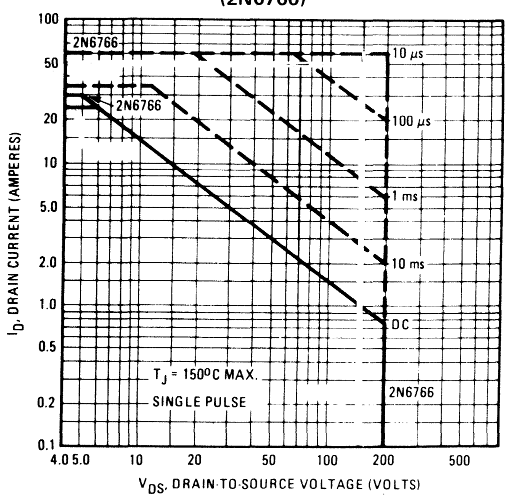


Fig. 8 — Maximum Safe Operating Area

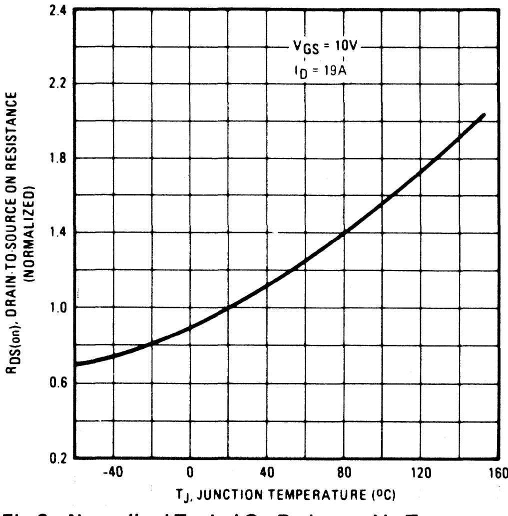


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

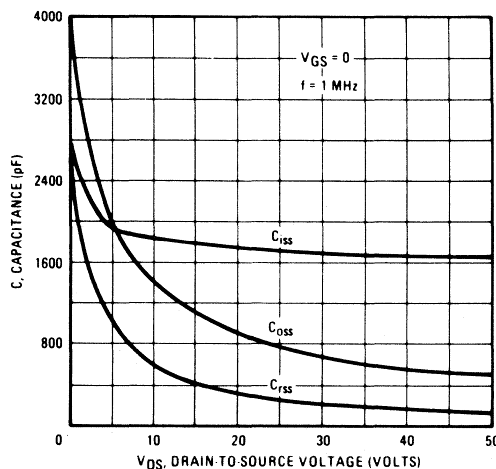


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

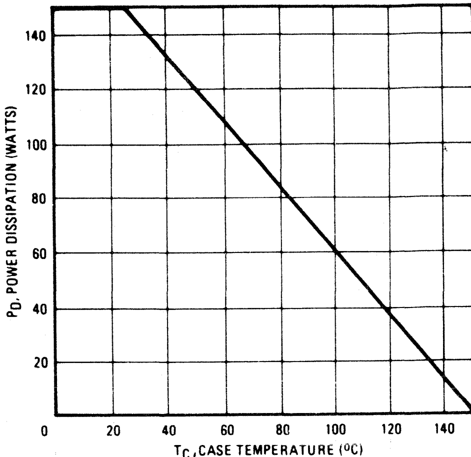


Fig. 11 — Power Vs. Temperature Derating Curve

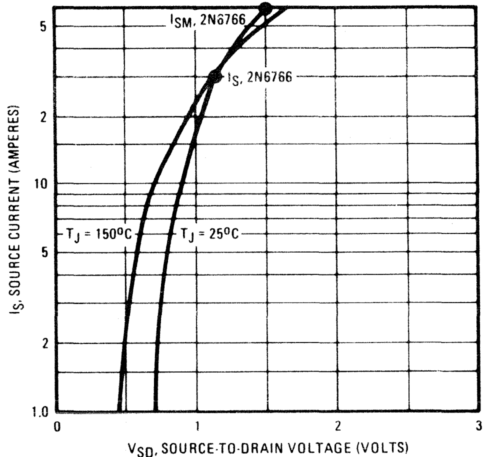


Fig. 12 — Typical Body-Drain Diode Forward Voltage

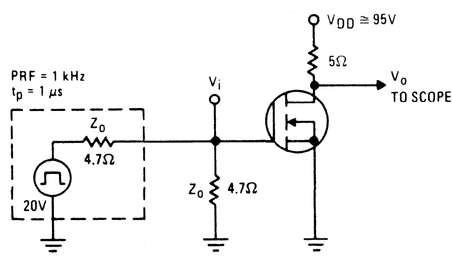


Fig. 13 — Switching Time Test Circuit

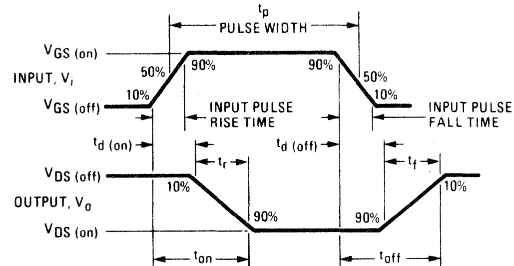


Fig. 14 — Switching Time Waveforms

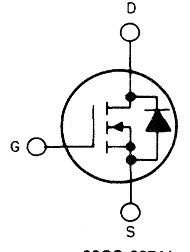
N-Channel Enhancement-Mode Power Field-Effect Transistors

3.5A, 100V

$r_{DS}(on) = 0.6\ \Omega$

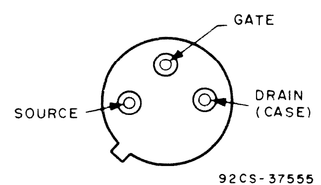
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-205AF

The 2N6782 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6782 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

Absolute Maximum Ratings

Parameter		2N6782	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.25*	A
I_{DM}	Pulsed Drain Current ③	14*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	3.50*	A
I_{SM}	Pulse Source Current (Body Diode) ③	14*	A
P_D @ T_C = 25°C	Max. Power Dissipation	15* (See Fig. 14)	W
	Linear Derating Factor	0.12* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 14	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	1000*	µA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	—	—	2.1*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	—	0.5	0.6*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 25°C
		—	—	1.08*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	—	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.0*	1.5	3.0*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	80	100*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	10*	20	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	15*	ns	V_{DD} ≅ 34V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	—	—	25*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	25*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	—	—	W	V_{DS} = 80V, I_D = 188 mA, See Fig. 16.
		15	—	—	W	V_{DS} = 4.28V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

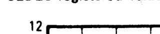
		Min.	Typ.	Max.	Units	
R_{thJC}	Junction-to-Case	—	—	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

		Value	Units	Test Conditions
t_{rr}	Reverse Recovery Time	200	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/µs
Q_{RR}	Reverse Recovered Charge	1.0	µC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/µs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value



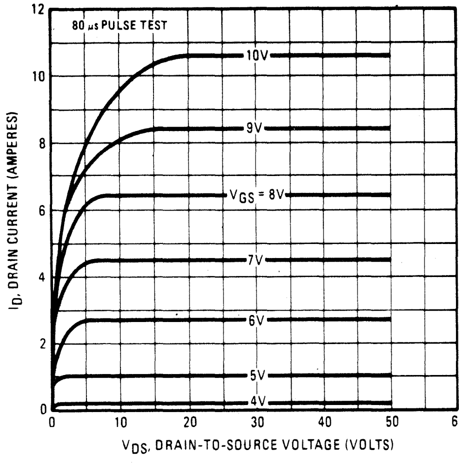


Fig. 1 — Typical Output Characteristics

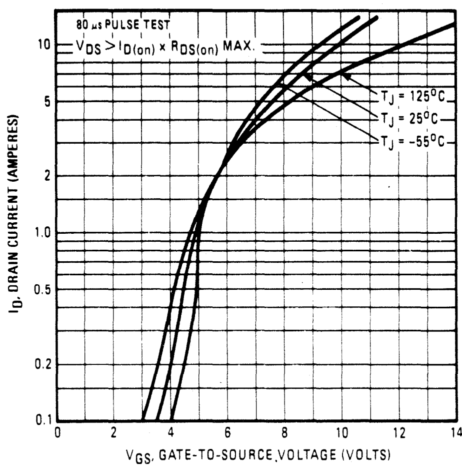


Fig. 2 — Typical Transfer Characteristics

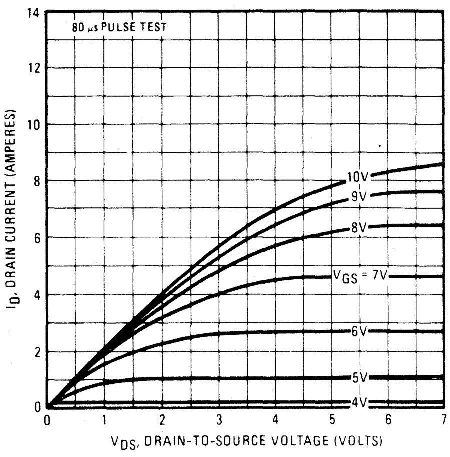


Fig. 3 — Typical Saturation Characteristics

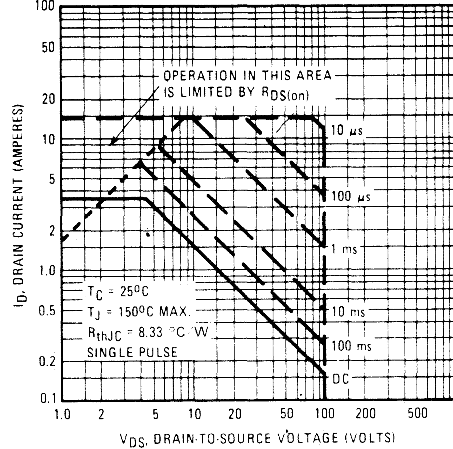


Fig. 4 — Maximum Safe Operating Area

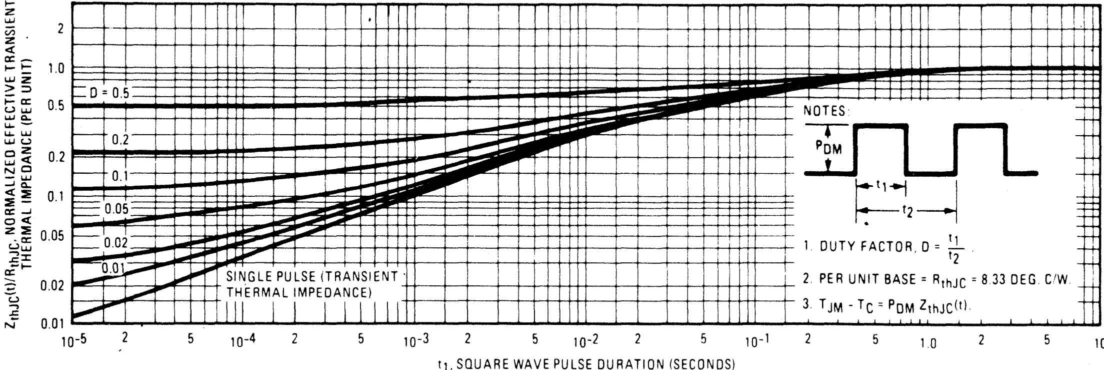


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

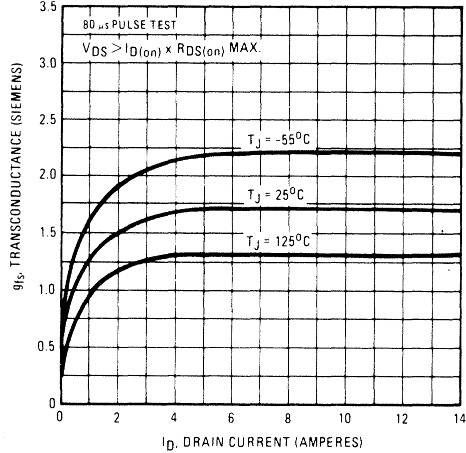


Fig. 6 — Typical Transconductance Vs. Drain Current

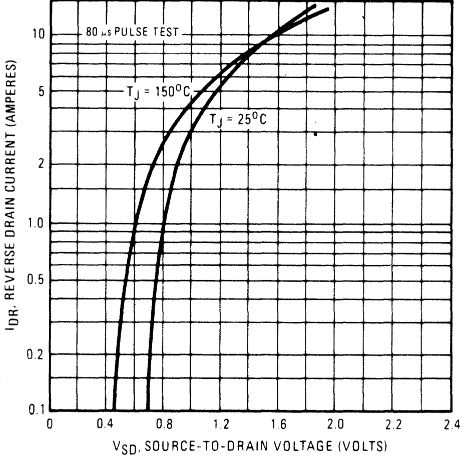


Fig. 7 — Typical Source-Drain Diode Forward Voltage

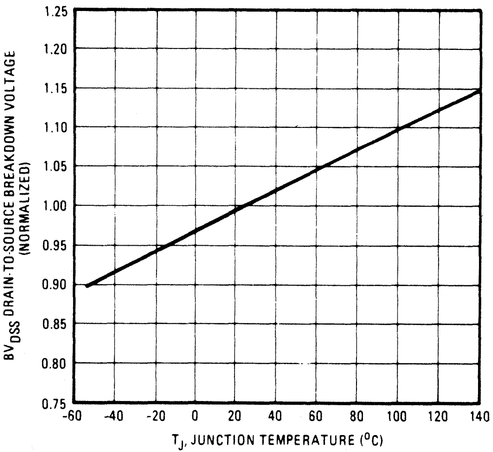


Fig. 8 — Breakdown Voltage Vs. Temperature

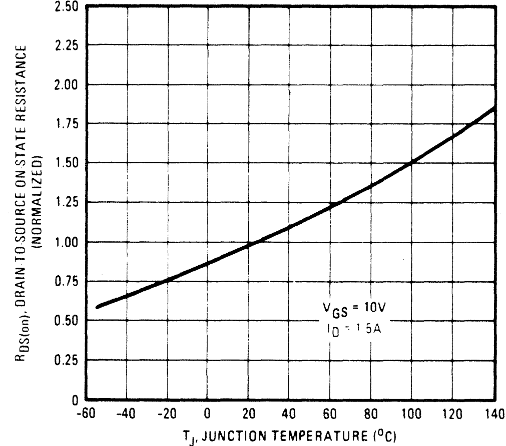


Fig. 9 — Normalized On-Resistance Vs. Temperature

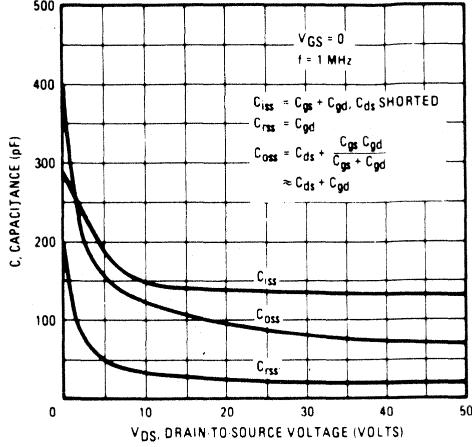


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

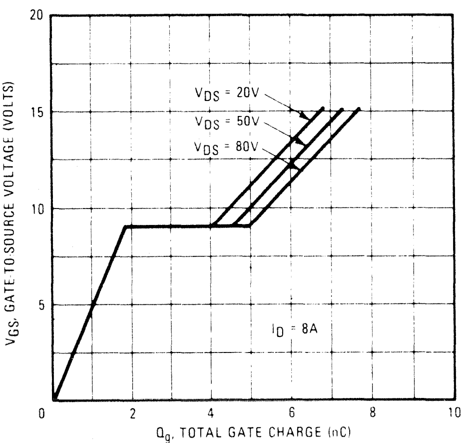


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

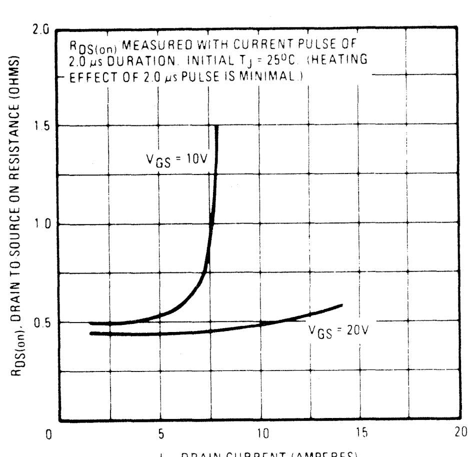


Fig. 12 — Typical On-Resistance Vs. Drain Current

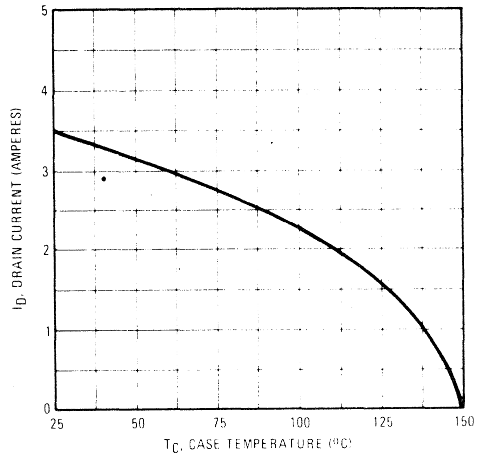


Fig. 13 — Maximum Drain Current Vs. Case Temperature

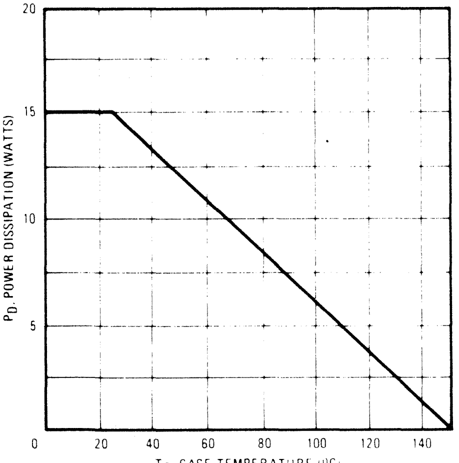


Fig. 14 — Power Vs. Temperature Derating Curve

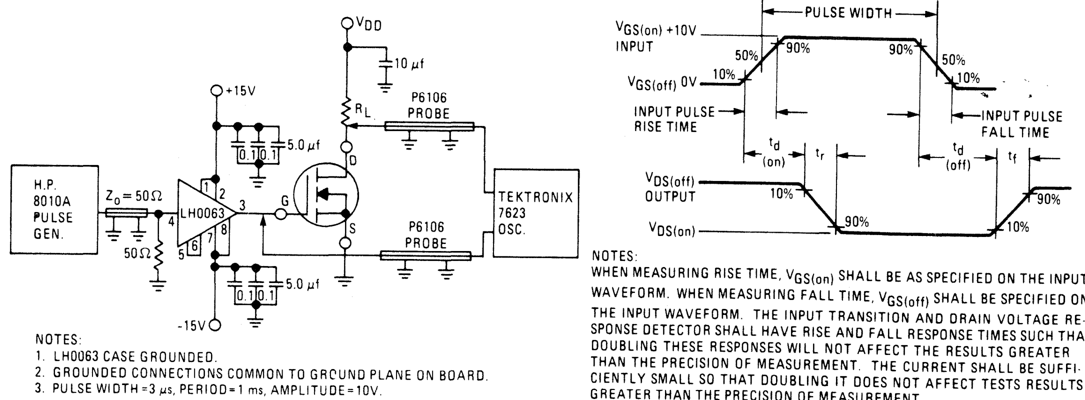


Fig. 15 — Switching Time Test Circuit

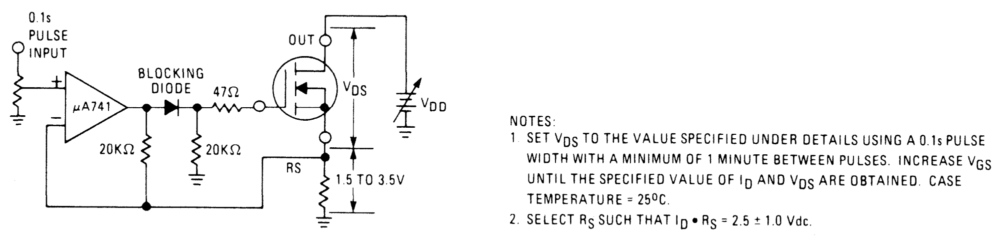


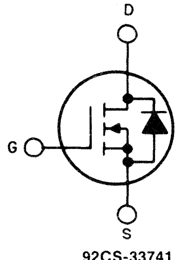
Fig. 16 — Safe Operating Area Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

6.0A, 100V

$r_{DS}(on) = 0.30\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

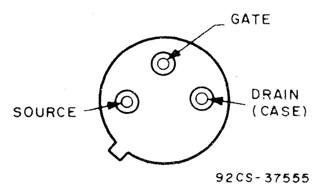


N-CHANNEL ENHANCEMENT MODE

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

TERMINAL DESIGNATIONS



JEDEC TO-205AF

Absolute Maximum Ratings

	Parameter	2N6788	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5*	A
I_{DM}	Pulsed Drain Current ③	24*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	6.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	24*	A
P_D @ T_C = 25°C	Max. Power Dissipation	20* (See Fig. 14)	W
	Linear Derating Factor	0.16* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 24	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	—	—	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	—	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		—	—	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	—	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.5*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40*	ns	V_{DD} ≅ 35V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	—	—	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	—	—	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	—	—	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.2	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

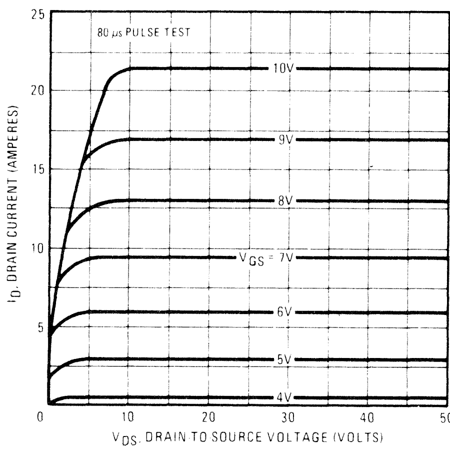


Fig. 1 — Typical Output Characteristics

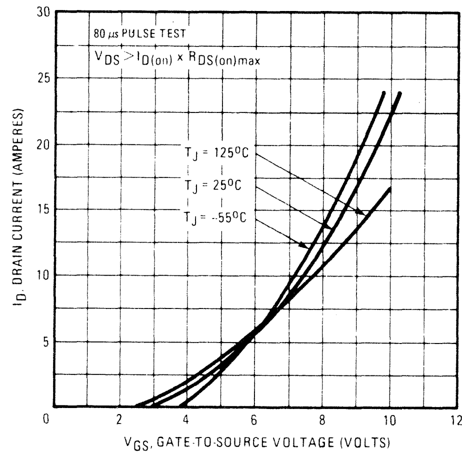


Fig. 2 — Typical Transfer Characteristics

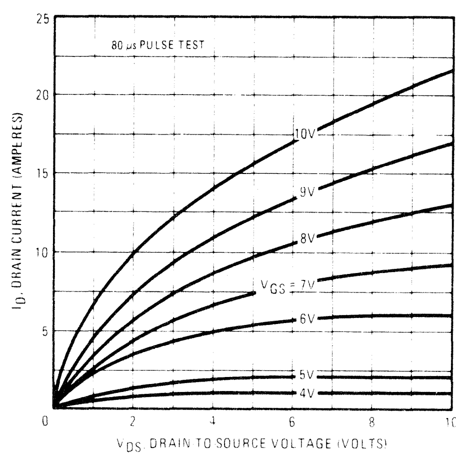


Fig. 3 — Typical Saturation Characteristics

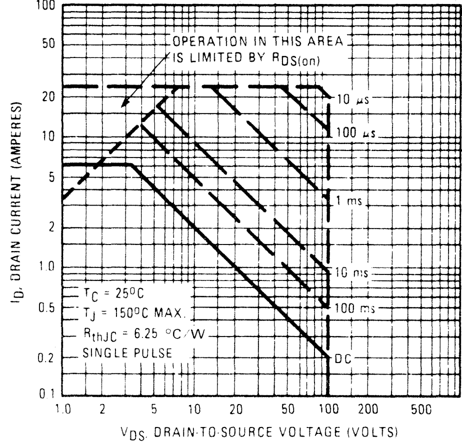


Fig. 4 — Maximum Safe Operating Area

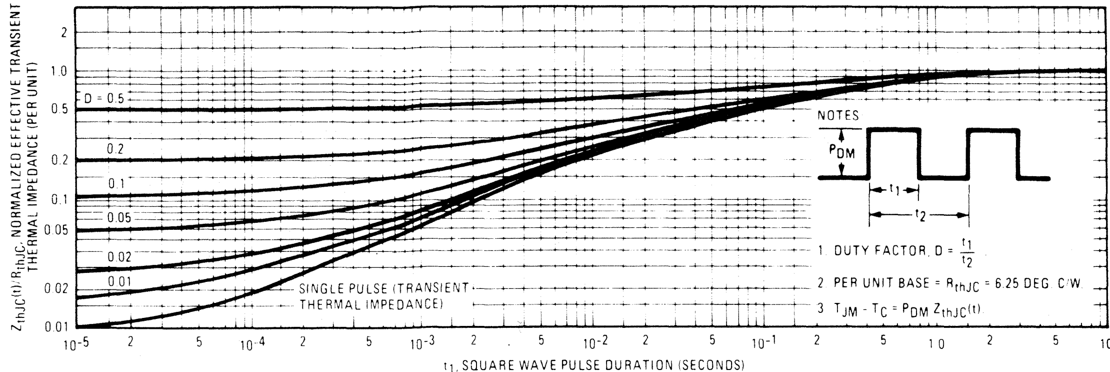


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

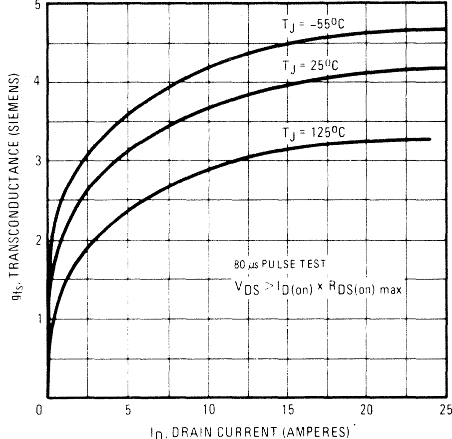


Fig. 6 – Typical Transconductance Vs. Drain Current

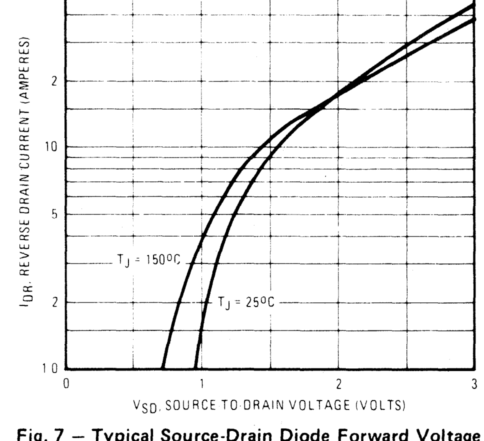


Fig. 7 – Typical Source-Drain Diode Forward Voltage

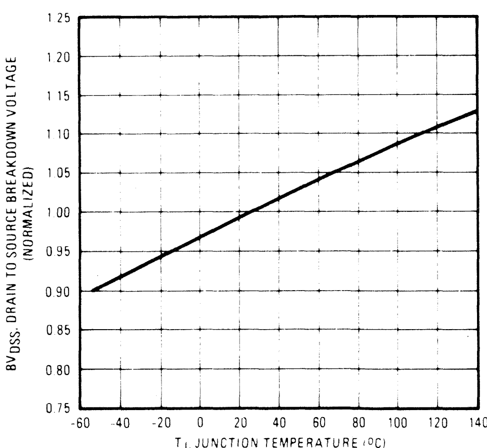


Fig. 8 – Breakdown Voltage Vs. Temperature

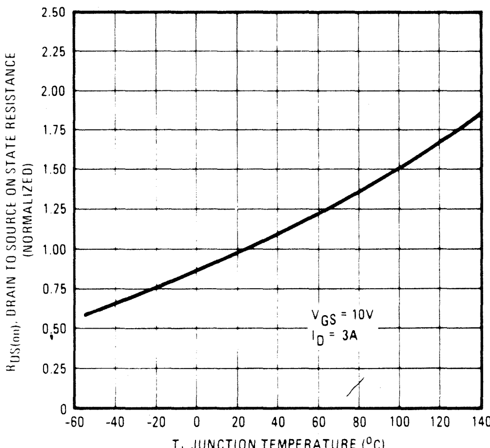


Fig. 9 – Normalized On-Resistance Vs. Temperature

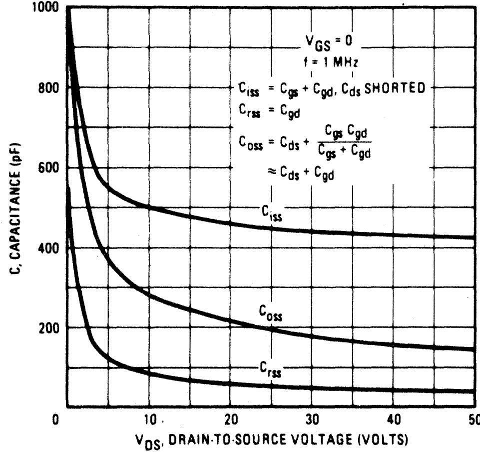


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

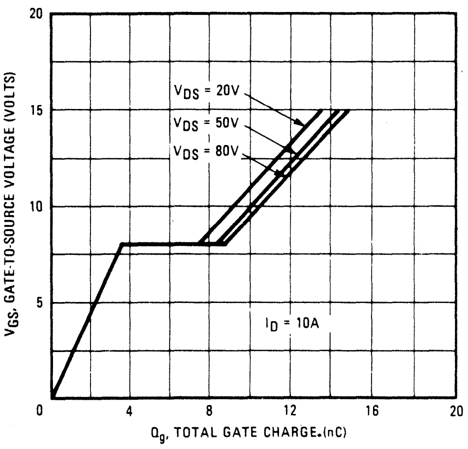


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

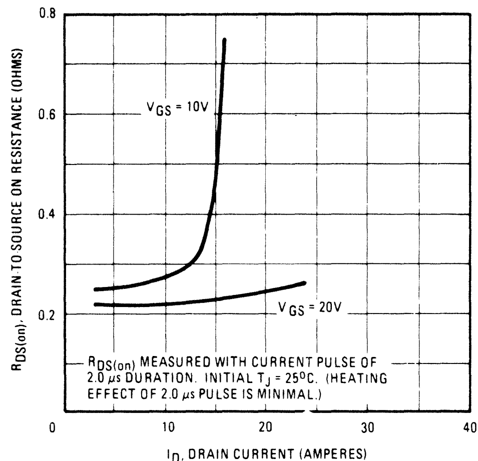


Fig. 12 – Typical On-Resistance Vs. Drain Current

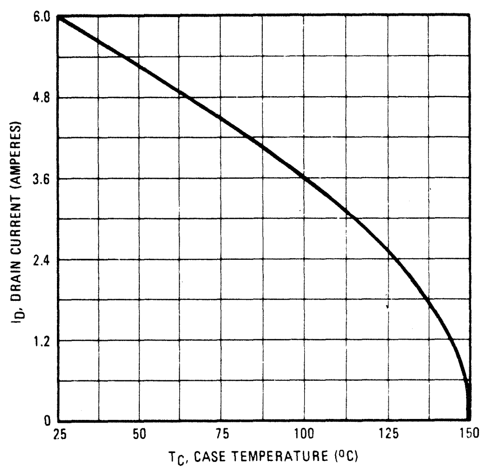


Fig. 13 – Maximum Drain Current Vs. Case Temperature

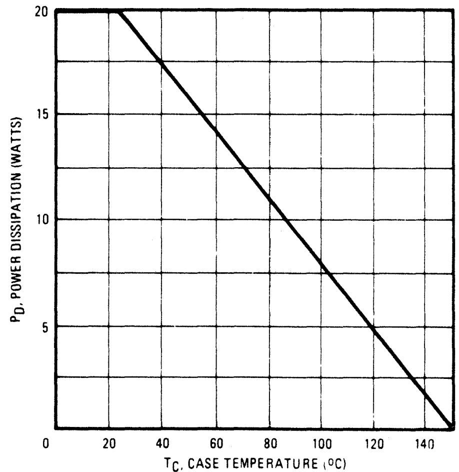


Fig. 14 – Power Vs. Temperature Derating Curve

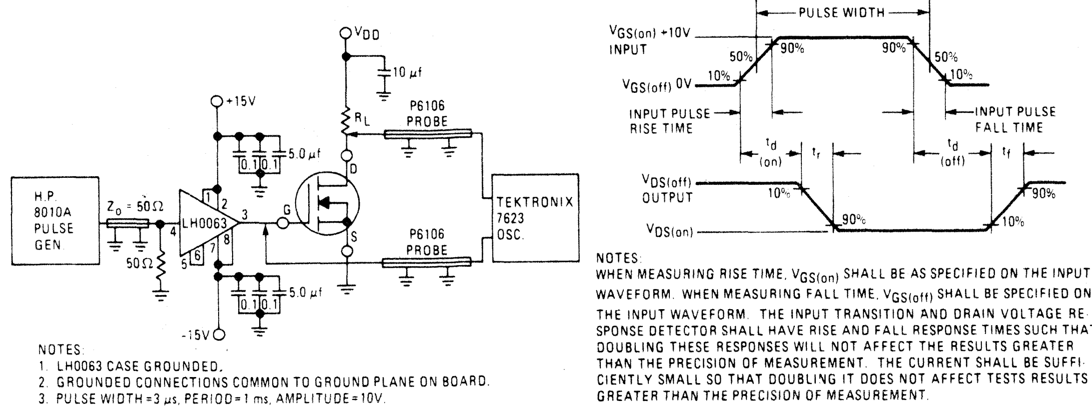


Fig. 15 – Switching Time Test Circuit

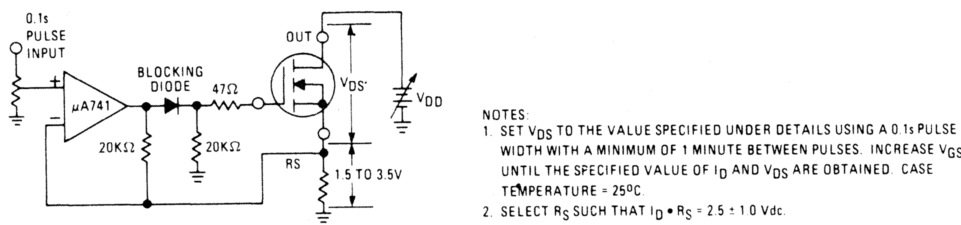


Fig. 16 – Safe Operating Area Test Circuit

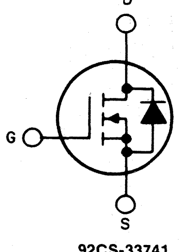
N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A, 100V

$r_{DS}(on) = 0.18\ \Omega$

Features:

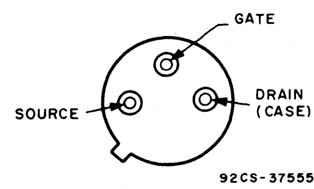
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



92CS-37555

JEDEC TO-205AF

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

Absolute Maximum Ratings

	Parameter	2N6796	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	A
I_{DM}	Pulsed Drain Current ③	32*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	8.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	32*	A
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.20* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	—	—	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	—	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		—	—	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	—	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(Ʊ)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_o = 50Ω
t_r	Rise Time	—	—	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	40*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	—	45*	ns	
SOA	Safe Operating Area	25	—	—	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	—	—	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ⩽ 300μs, Duty Cycle ⩽ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

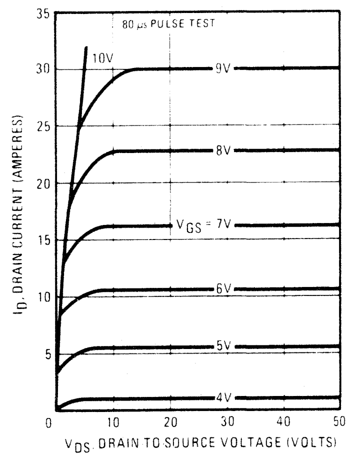


Fig. 1 — Typical Output Characteristics

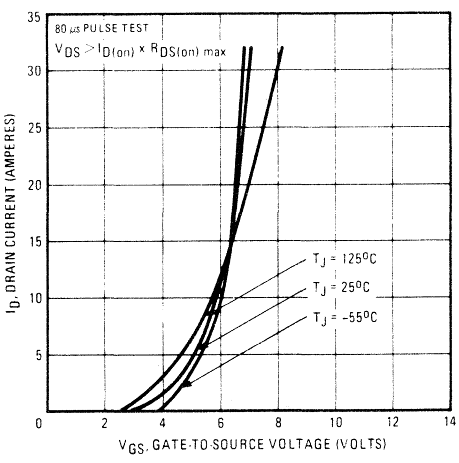


Fig. 2 — Typical Transfer Characteristics

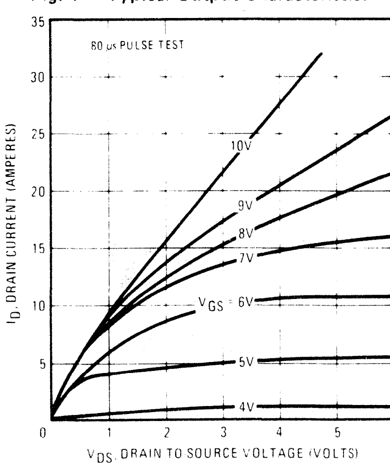


Fig. 3 — Typical Saturation Characteristics

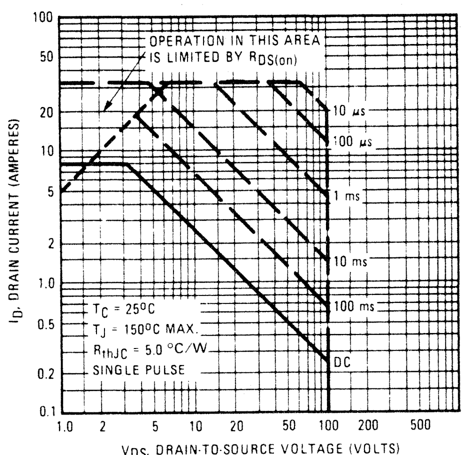


Fig. 4 — Maximum Safe Operating Area

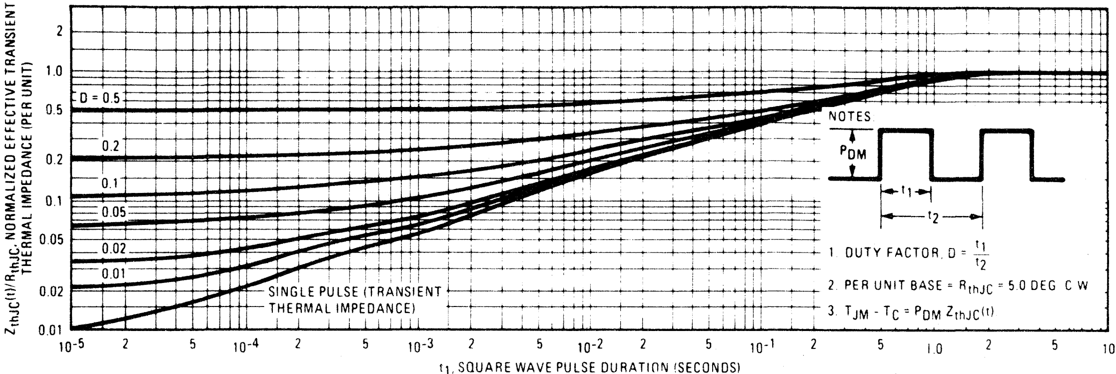


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

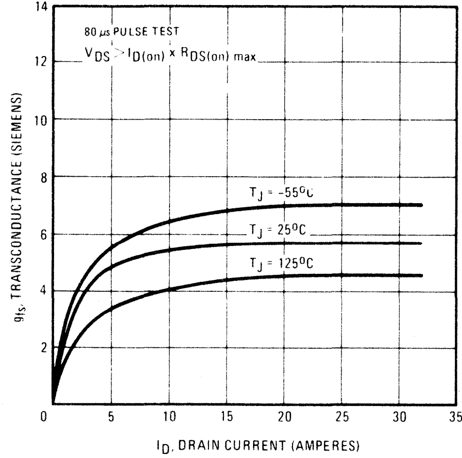


Fig. 6 — Typical Transconductance Vs. Drain Current

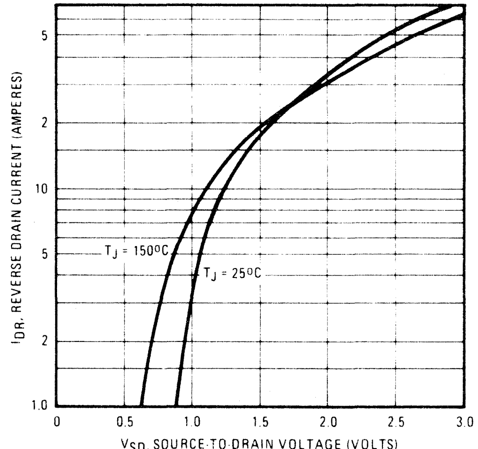


Fig. 7 — Typical Source-Drain Diode Forward Voltage

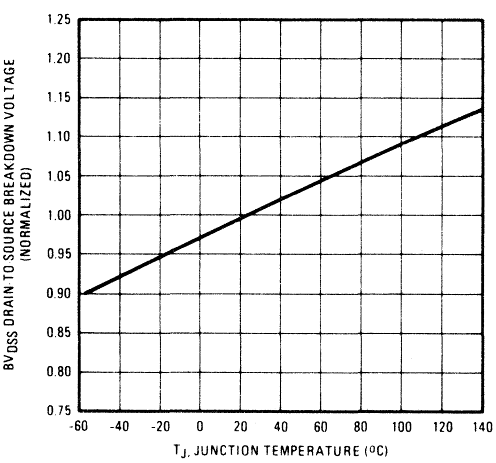


Fig. 8 — Breakdown Voltage Vs. Temperature

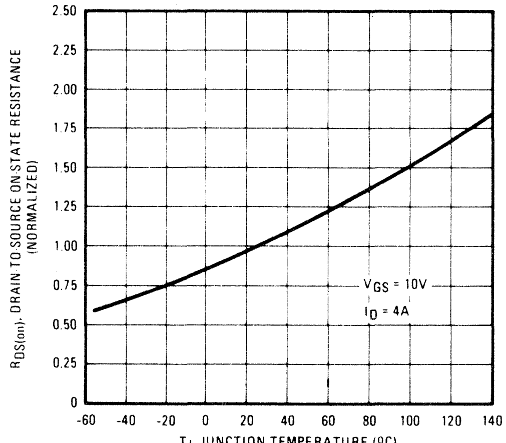


Fig. 9 — Normalized On-Resistance Vs. Temperature

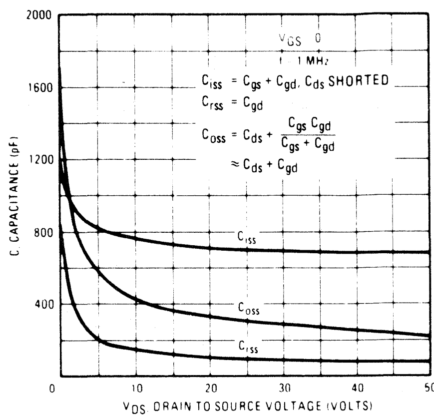


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

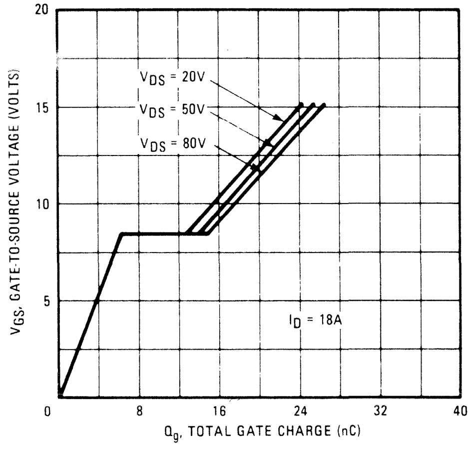


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

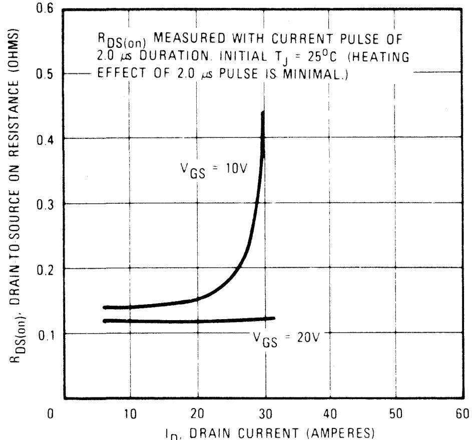


Fig. 12 — Typical On-Resistance Vs. Drain Current

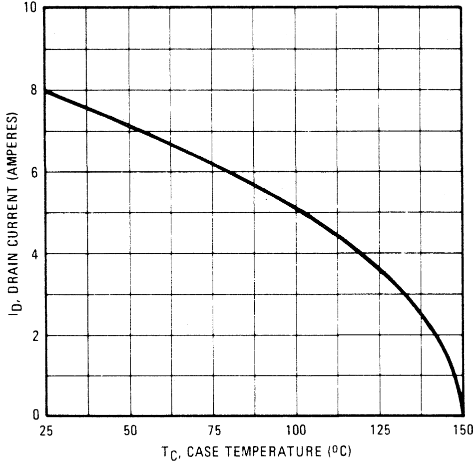


Fig. 13 — Maximum Drain Current Vs. Case Temperature

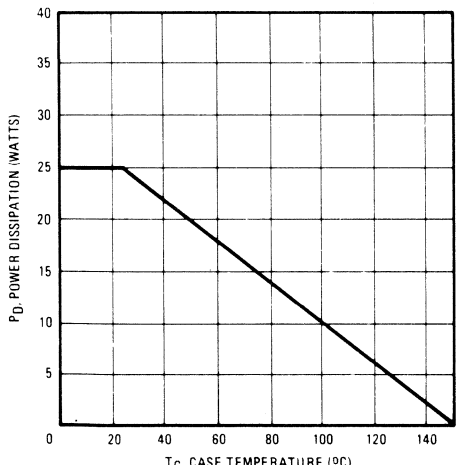


Fig. 14 — Power Vs. Temperature Derating Curve

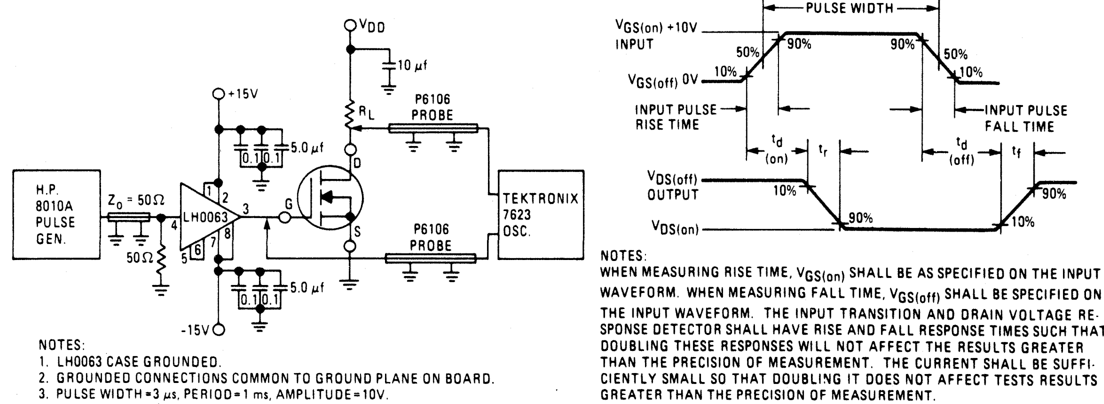


Fig. 15 — Switching Time Test Circuit

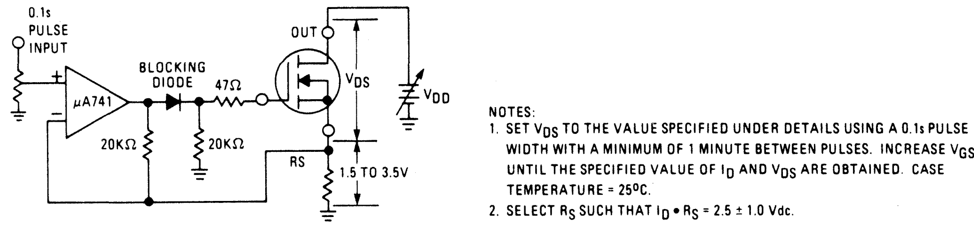
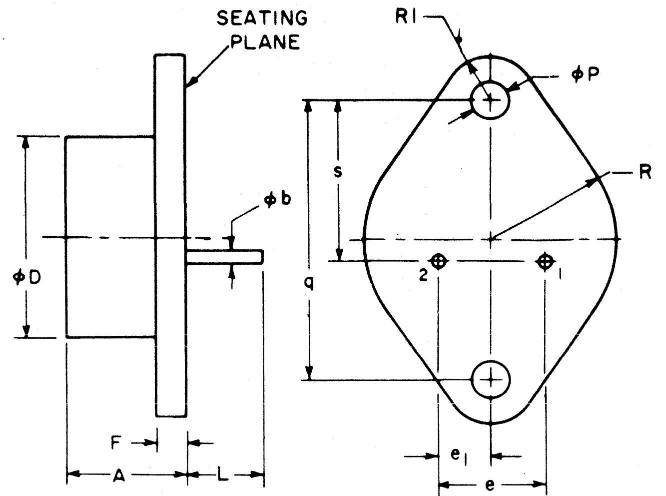


Fig. 16 — Safe Operating Area Test Circuit

JEDEC TO-204AA



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.038	0.043	0.966	1.092	
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	—	0.135	—	3.42	
L	0.312	—	7.93	—	
φP	0.151	0.161	3.84	4.08	
q	1.187	BSC	30.15	BSC	
R	—	0.525	—	13.33	
R_1	—	0.188	—	4.77	
s	0.655	0.675	16.64	17.14	

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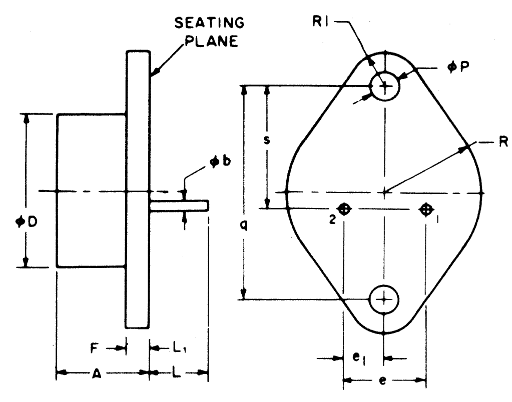
JEDEC TO-204AE

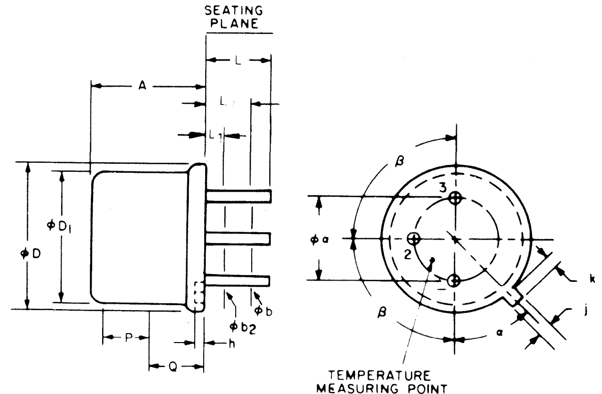


SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	**0.250**	**0.450**	**6.4**	**11.4**	
φb	**0.057**	**0.063**	**1.45**	**1.60**	
$φD_2$	**—**	**0.875**	**—**	**22.22**	
e	**0.420**	**0.440**	**10.67**	**11.17**	
e_1	**0.205**	**0.225**	**5.21**	**5.71**	
F	**0.060**	**0.135**	**1.53**	**3.42**	
L	**0.440**	**0.480**	**11.18**	**12.19**	
φP	**0.151**	**0.161**	**3.84**	**4.08**	
q	**1.187**	**BSC**	**30.15**	**BSC**	
R	**0.495**	**0.525**	**12.58**	**13.33**	
R_1	**0.131**	**0.188**	**3.33**	**4.77**	
s	**0.655**	**0.675**	**16.64**	**17.14**	

92CS-36443

Dimensional Outlines

JEDEC TO-205AF



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	.200 BSC		5.08 BSC		4
A	.160	.180	4.07	4.57	
ϕb	.016	.021	.41	.53	5
ϕb_2	.016	.019	.41	.48	5
ϕD	.340	.370	8.64	9.39	
ϕD_1	.315	.355	8.01	9.01	2
h	.009	.041	.23	1.04	
j	.028	.034	.72	.86	
k	.029	.045	.74	1.14	1
L	.500	.750	12.70	19.05	5
L_1	—	.050	—	1.27	5
L_2	.250	—	6.35	—	5
P	.070	—	1.78	—	2
Q	—	.050	—	1.27	3
α	45° NOMINAL		—	—	
β	90° NOMINAL		—	—	

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Notes:

1: Dimension k measured from ϕD maximum.

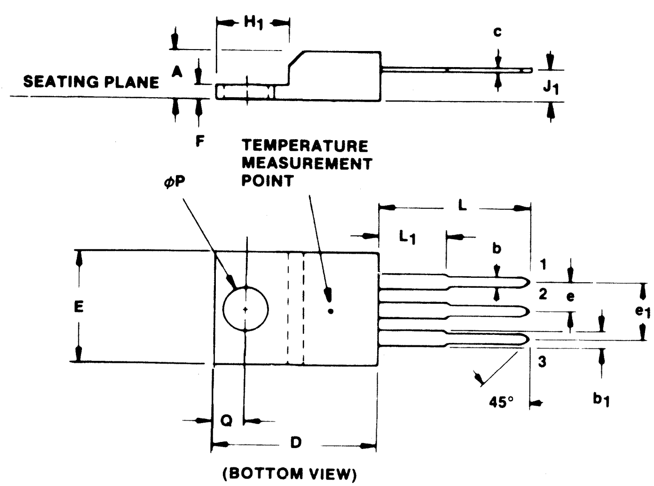
2: ϕD_1 shall not vary more than .010 in Zone P. This zone controlled for automatic handling.

3: Details of outline in this zone optional.

4: Leads at gauge plane .054-.055 below seating plane shall be within .007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.

5: ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

JEDEC TO-220AB



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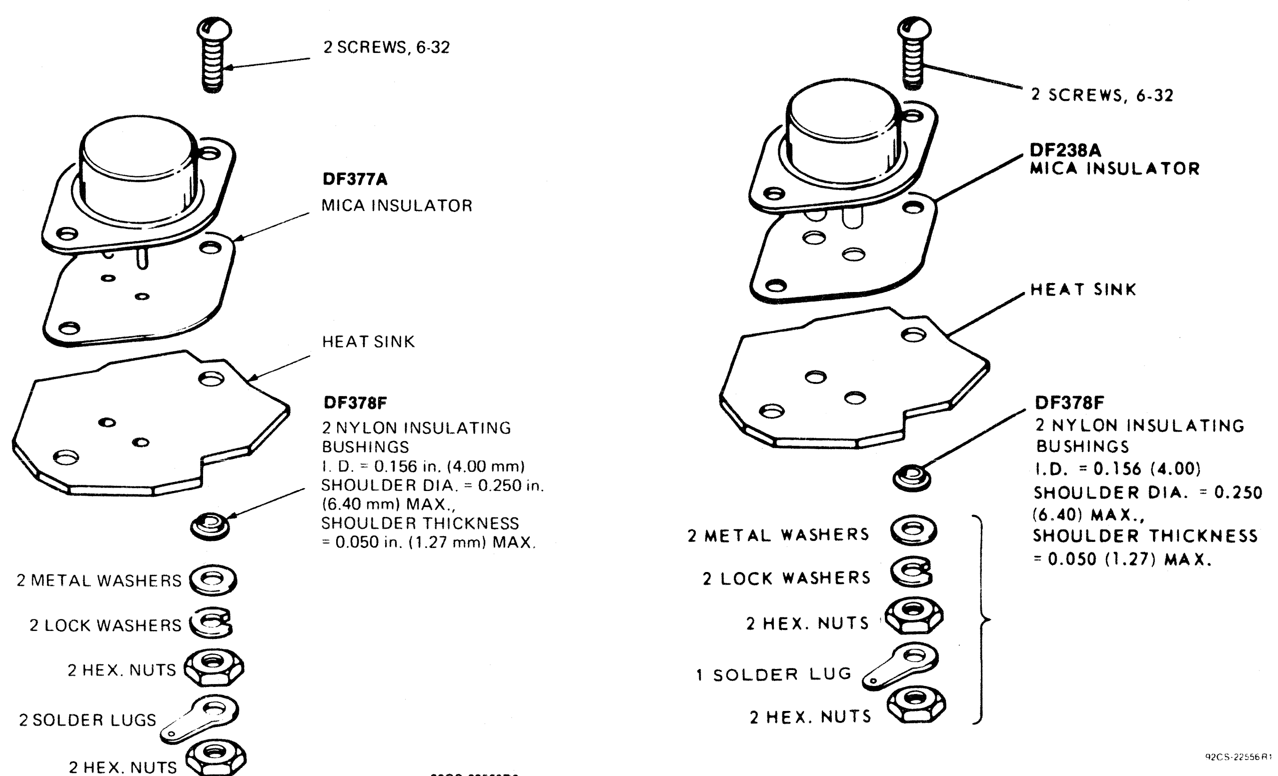
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.140	0.190	3.56	4.82
b	0.020	0.045	0.51	1.14
b_1	0.045	0.070	1.14	1.77
c	0.015	0.025	0.38	0.63
D	0.560	0.625	14.23	15.87
E	0.380	0.420	9.66	10.66
e	0.090	0.110	2.29	2.79
e_1	0.190	0.210	4.83	5.33
F	0.045	0.055	1.14	1.39
H_1	0.230	0.270	5.85	6.85
J_1	0.080	0.115	2.04	2.92
L	0.500	0.562	12.70	14.27
L_1	—	0.250	—	6.35
ϕP	0.139	0.161	3.531	4.089
Q	0.100	0.120	2.54	3.04

NOTES:

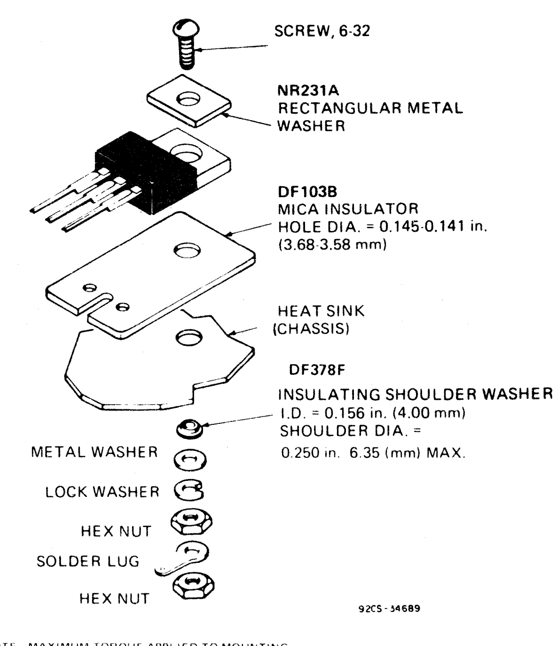
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 — 0.255 in. (6.350 — 6.477 mm) from case.

Mounting Hardware



Suggested mounting hardware for JEDEC TO-204AA (formerly JEDEC TO-3)

Suggested mounting hardware for JEDEC TO-204AAE (formerly JEDEC TO-3)



NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8 in. lb. (0.09 kgf m)

Suggested mounting hardware for JEDEC TO-220AB

Sales Offices

United States

Alabama
RCA
303 Williams Avenue,
Suite 133
Huntsville, AL 35801
Tel: (205) 533-5200

Arizona
RCA
6900 E. Camelback Road, Suite 460, Scottsdale, AZ 85251
Tel: (602) 947-7235

California
RCA
3150 De La Cruz Blvd.
Bldg. D, Suite 206
Santa Clara, CA 95050
Tel: (408) 748-0933

RCA
4827 No. Sepulveda Blvd., Suite 420, Sherman Oaks, CA 91403
Tel: (213) 468-4200

RCA
17731 Irvine Blvd., Suite 104
Magnolia Plaza Bldg.
Tustin, CA 92680
Tel: (714) 832-5302

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RCA Corp.
6767 So. Spruce Street
Englewood, CO 80112
Tel: (303) 740-8441

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P.O. Box 12247
Lake Park, FL 33403
Tel: (305) 626-6350

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RCA
Suite 304
2872 Woodcock Blvd.
Atlanta, GA 30341
Tel: (404) 452-2355

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2700 River Road
Des Plaines IL 60018
Tel: (312) 391-4380

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9240 N. Meridian Street,
Indianapolis, IN 46260
Tel: (317) 267-6375

Kansas
RCA
8900 Indian Creek Parkway
Suite 410
Overland Park, KS 66210
Tel: (913) 642-7656

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20 William Street,
Wellesley, MA 02181
Tel: (617) 237-7970

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30400 Telegraph Road,
Birmingham, MI 48010
Tel: (313) 644-1151

Minnesota
RCA
6750 France Avenue, So., Suite 122, Minneapolis, MN 55435
Tel: (612) 929-0676

New Jersey
RCA
1998 Springdale Road
Cherry Hill, NJ 08003
Tel: (609) 338-5042

RCA
67 Walnut Avenue
Clark, NJ 07066
Tel: (201) 574-3550

New York
RCA
160 Perinton Hill Office Park
Fairport, NY 14450
Tel: (716) 223-5240

Ohio
RCA
6600 Busch Blvd., Suite 110
Columbus, OH 43229
Tel: (614) 436-0036

Texas
RCA
17000 Dallas Parkway
Suite 100
Dallas, TX 75248-1921
Tel: (214) 733-0800

Virginia
RCA
1901 N. Moore Street
Arlington, VA 22209
Tel: (703) 558-4161

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3501 29th Street, NE
Calgary, Alberta T1Y 5W4
Tel: (403) 291-1469

Ontario
RCA Inc.
1 Vulcan Street, Rexdale
Ontario M9W 1L3
Tel: (416) 247-5491

Ontario Cont'd
RCA Inc.
411 Roosevelt Avenue
Suite 203A, Ottawa
Ontario K2A 3X9
Tel: (613) 728-0031

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Tel: 02/720.89.80

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78140 Velizy
Tel: (3) 946.56.56

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8000 Munchen 2
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Tsimshatsui, Kowloon
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37 Mori Building
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Solid State Division, 24-15 International Plaza, 10 Anson Road
Singapore 0207
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Ramiro E. Podetti Reps.
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SID Distribuidora De Componentes LTDA
Av. Brig Faria Lima 1476
7th Floor, Sao Paulo 01452
Tel: (011) 210-4033

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